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THESIS

RELIABILITY AND CHARACTERIZATION OF HIGH VOLTAGE POWER CAPACITORS

by

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March 2014

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Alternative energy products are an increasingly common sight on military bases in the United States. Energy product reliability affects the sustainability and cost-effectiveness of these systems, which must be tested by outside entities to ensure quality.

The purpose of this thesis is to perform component level reliability testing on a high voltage power capacitor used in an electrical vehicle solar charging system. A component level characterization was performed to better understand the physical attributes of these capacitors. This investigation identified the expected component lifetime and conditions in which this component will become less reliable. Results are compared to those published by the manufacturer.

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RELIABILITY AND CHARACTERIZATION OF HIGH VOLTAGE POWER CAPACITORS

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ABSTRACT

Alternative energy products are an increasingly common sight on military bases in the United States. Energy product reliability affects the sustainability and cost-effectiveness of these systems, which must be tested by outside entities to ensure quality.

The purpose of this thesis is to perform component level reliability testing on a high voltage power capacitor used in an electrical vehicle solar charging system. A component level characterization was performed to better understand the physical attributes of these capacitors. This investigation identified the expected component lifetime and conditions in which this component will become less reliable. Results are compared to those published by the manufacturer.

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LIST OF ACRONYMS AND ABBREVIATIONS

A	amperes
a	area
AC	alternating current
BNC	Bayonet Neill Concelman
C	capacitor
c	capacitance
d	distance
DoD	Department of Defense
ε	permittivity
EVCS	electric vehicle charging system
GPIB	general-purpose interface bus
GW	giga-watt
HVST	high voltage stress test
IV	current voltage plot
IPC	Ideal Power Converters
LabVIEW	Laboratory Virtual Instrument Engineering Workbench
MHz	mega-hertz
nF	nano-farads
N_t	Concentration of traps
pA	pico-amps
PCB	printed circuit board
PP	polypropylene
q	charge of an electron
Q_{TFL}	excess carrier charge density
R	resistor
R^2	coefficient of determination
R_k	resistor at the kth term
RF	radio frequency
Si	silicon
T	time

μm	micrometer
μs	microseconds
V	voltage
V_k	voltage of the kth term
V DC	voltage direct current
VI	virtual instruments
V_{TFL}	trap-filled limit voltage

EXECUTIVE SUMMARY

The purpose of this thesis is to address the need for reliable alternative energy devices, specifically designed for use on military bases. Two issues are addressed in this work. The first investigation proposes a different method to characterize thin film capacitor degradation, using the principles developed for semiconductors. The second determines whether these capacitors have the stated reliability characteristic provided by the manufacturer. The goal of this system reliability study is to allow the military to install a long-term alternative energy system, reducing the militaries dependence on traditional fossil fuel.

The typical solar power system requires multiple subsystems as well as the physical infrastructure to support the solar panels. The solar energy absorbed from the sun is converted by the power converter unit and then is converted into a usable form for use in an electric vehicle. This thesis will address the alternating current (AC) link converter used in the construction of the solar power system, manufactured by Ideal Power Converter (IPC). This converter is being used for the Electric Vehicle Charging Station (EVCS), currently being investigated and installed in Port Hueneme, CA, as part of the DoD shift to renewable energy on military installations.

The capacitors used for this thesis are used in two testing phases. Phase one considers the characterization of thin film capacitors by developing Current-Voltage (IV) curves of each capacitor at various voltages. Characterization is performed using the methodology normally reserved for semiconductors. Phase two develops a high voltage stress test (HVST), to investigate the usable lifetime of the capacitor.

Electron traps and material defects play a significant role in affecting current injection in semiconductor. The following image depicts the characteristics of space charged limited current, which are evident in the material during the characterization process of this thesis. This figure provides for a graphical understanding of the IV characteristic that shifts from a Ohmic relationship to a square law relationship as the material is altered by the internal electron injection traps.

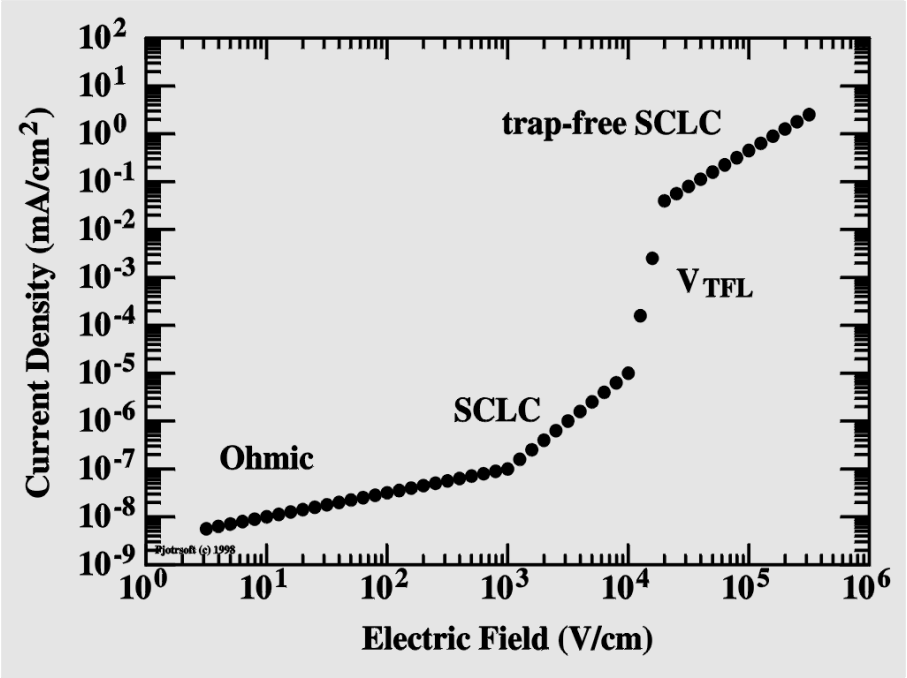

Figure 1. Log-log plot of current density versus electric field to showcase the change in the current-voltage relationship due to a material with electron injection traps.

For the characterization testing, the applied test voltage was measured from 0V to 500V, in incremental steps of 50V. Every two seconds, the voltage across the resistor was measured and then recorded. Each step of voltage was tested for a testing duration of 2000 seconds and an average value was calculated over the last 100 data points taken. All characterization testing was accomplished at room temperature, 25 degrees Celsius. The data was averaged to get for an accurate value of the voltage measured.

The high voltage stress test required the capacitors to be tested until a significant change was seen in the capacitance value of the capacitor. Generally, a negative drop in the capacitance value of two to five percent predicts a capacitor that is degrading enough to require the capacitor to be replaced. To accomplish this type of testing the capacitor must be exposed to a much higher voltage or temperature, or to test the capacitor at rated voltage for the expected lifetime. Due to time constrains, it was not feasible to test the capacitors at rated voltage for 100000 hours to determine if they would fail. Instead, the principle of excessive temperature/voltage was used.

The characterization data was placed on a log-log plot to showcase the SCL current and PF effect during the testing. Due to high background noise, a copper-clad box was designed and tested in the same manner as the PCB circuit board for characterization analysis.

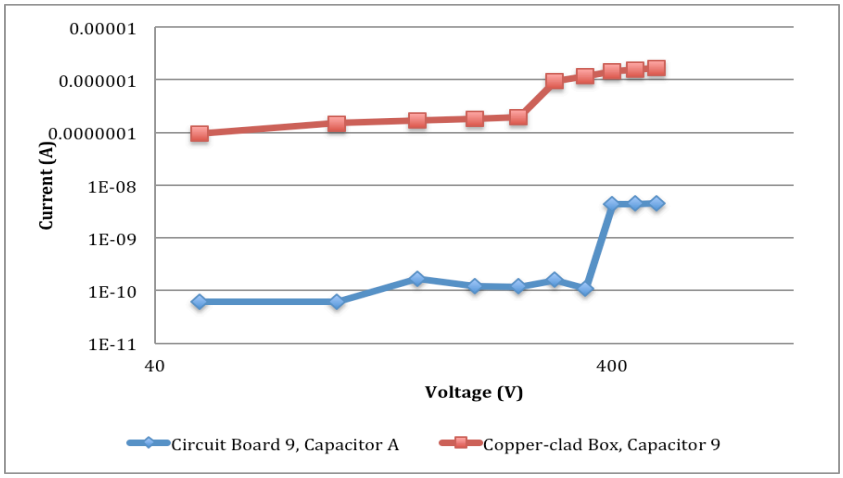

Figure 2 Log-log plot of zeroed current versus test voltage from PCB circuit board and copper-clad box depicting the change in current as voltage is incrementally increased.

The IV plot shown in Figure 2 was then compared to that shown in Figure 1, which depicts rise in voltage density due to the effects of SCLC with the PF effect. The figure illustrates the rise in current between 350V DC and 400 V DC for the PCB circuit board and 250V DC and 300V DC for the copper-clad box.

This overall trend is that of a power law relationship between the current and voltage, which is what is expected. Fluctuations in the power law in the PCB circuit board are due to the excessive noise that was present in the laboratory-testing environment. The rise in current for the copper-clad box is due to a change in the low pre-noise amplifier, which was recalibrated prior to the copper-clad box testing. It can also be seen that the use of the copper-clad box and air connection method can minimize the external noise, specifically when using a recalibrated amplification measurement circuit.

Lifetime reliability testing was performed on one PCB circuit board. The lifetime reliability data were placed on a linear plot, shown in Figure 3, to provide the relationship between the measured capacitance value and the length of time during which the capacitor was stressed during testing.

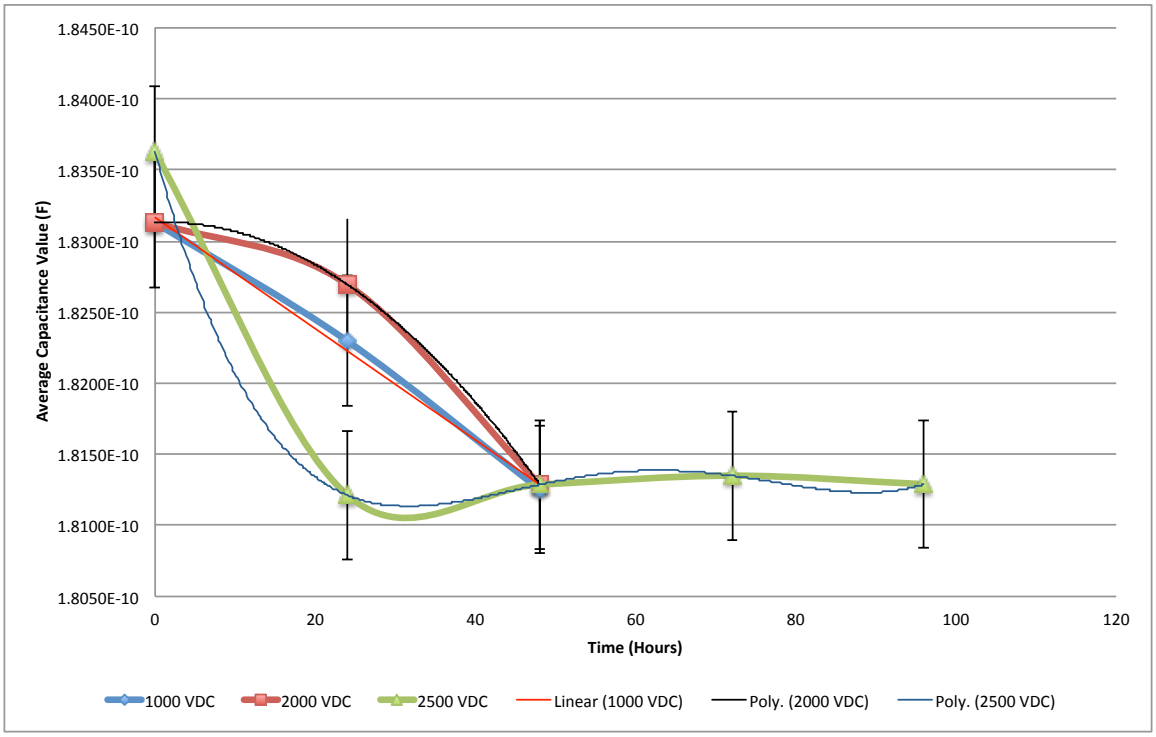

Figure 3. Linear plot of measured capacitance value versus length of time in which the capacitor was stressed. The trend lines used for the extrapolation data come from this plot and indicate the expected lifetime at each test voltage.

Due to length of time required for a lifetime reliability test, the lifetime reliability data had to be extrapolated. The extrapolation method is a proven method used in other lifetime reliability testing when the time allowed for testing is limited. Extrapolated lifetime data are not as accurate as the continued lifetime testing data, but it gives the expected lifetime of the capacitor under similar operating conditions with a certain variance. The extrapolated lifetime reliability calculations at each test voltage are provided in Table 1.

Table 1 Extrapolated data used to compare the measured lifetime reliability to the expected lifetime reliability provided by the capacitor manufacturer.

Test Voltage	R^2 Value	Trendline Equation	Capacitor Lifetime (Years)
1000 VDC	1	$C=-4\ 10^{-14}\ T+2\ 10^{-10}$	8.22
2000 VDC	0.99587	$C = -8\ 10^{-16}T^2 + 2\ 10^{-15}T + 2\ 10^{-10}$	2.15
2500 VDC	1	$C=3\ 10^{-19}T^4 – 7\ 10^{-17}T^3 + 6\ 10^{-15}T^2 – 2\ 10^{-13}T + 2\ 10^{-10}$	0.98

The manufacturer data sheet states that the capacitor lifetime at 1500V DC, and a temperature of 70 degrees Celsius is 11 years. The capacitance value obtained using the extrapolation method for all three stress tests provided a lifetime of less than 11 years.

Due to the limited amount of time to collect the lifetime reliability data, the best fit for these data sets was determined on a case-by-case basis. This was determined using the coefficient of determination, R^2. When R^2 is as close to one as possible, the trend line indicates an accurate representation of the data plotted. For the 1000V DC test, a linear tread line was used due to R^2 being equal to one for this datum set. For the 2000V DC stress condition, a second order polynomial was used since the coefficient of determination, R^2, is as close to one as possible. A fourth order polynomial trend line was determined to be the best fit for the 2500V DC stress testing datum set since R^2 was equal to 1.

At 2500V DC, a variation in the capacitance value was observed, as depicted in Figure 3. The capacitance value leveled off at the 48-hour mark and did not decrease as the capacitor continued to be stressed. This is believed to be an indication of the self-healing process that occurs in thin film capacitors. During self-healing, a small portion of the total capacitance is removed. This occurs only in areas where material defects are present. For this capacitor, self-healing occurred during the initial 48 hours testing. Once these material defects were removed, the capacitance value remained constant. The overall change in the capacitance value due to the self-healing is within one percent of the initial value.

Since all capacitors tested have the same material properties, it can be said that if time were available, the same trend of self-healing would be visible for the 1000V DC test condition and the 2000V DC condition. Analyzing the test results after the initial 48

hours of testing, the capacitors were shown to be relatively robust in design. Results show that once the initial defects are removed due to the self-healing process, the capacitance value is constant even at an elevated temperature and voltage.

The development of this alternative characterization method of these capacitors provides a better understanding of their degradation behavior over time at a material science level. These results will also aid in the ability of the Department of Defense to procure the best alternative energy systems available for use on military installations.

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I. INTRODUCTION

A. PURPOSE

In 2012, President Barack Obama announced in his State of the Union address that the Department of Defense would purchase or facilitate the production of 1 gigawatt (GW) of renewable energy for use on Navy and Marine Corps installations [1]. As part of this directive, the U.S. will be installing solar power systems to aid in reducing the amount of energy consumed by our military bases.

Systems reliability is important in predicting the expected lifetime and operating parameters required to ensure these solar systems last as long as advertised by manufacturers. System reliability is described as the ability of a system or component to perform its required functions under stated conditions for a specified period of time [2]. As solar systems become integrated into our military bases, it is imperative to ensure that these systems are reliable. Installing an un-reliable system would be far more detrimental in the long term than if the system was never installed, both in terms of mission accomplishment and overall lifetime costs. This would lead into a domino type effect, where a significant number of individuals and companies would be impacted by the failure of a single entity.

The purpose of this thesis is to evaluate the reliability of the critical component of a commercial solar inverter, the thin film capacitor element. Two issues will be considered in this work. The first investigation proposes a different method to characterize thin film capacitor degradation, using the principles developed for semiconductors. The second determines whether these capacitors have the stated reliability characteristic provided by the manufacturer. This reliability study will contribute to the effects towards installing a proper alternative energy system that will last, reducing the militaries overall dependence on traditional fossil fuel.

B. CONVERTER OVERVIEW

The typical solar power system requires multiple subsystems as well as the physical infrastructure to support the solar panels. The solar energy absorbed from the

sun is converted by the power converter unit to a usable form for use in applications such as electric vehicle battery charging. This thesis addresses only the alternating current (AC) link converter used in the construction of the solar power system, specifically the Ideal Power Converter (IPC) AC link converter being used for the Electric Vehicle Charging Station (EVCS) shown in Figure 1. This converter is currently being investigated and installed in Port Hueneme, CA as part of the DoD shift to renewable energy on military installations.

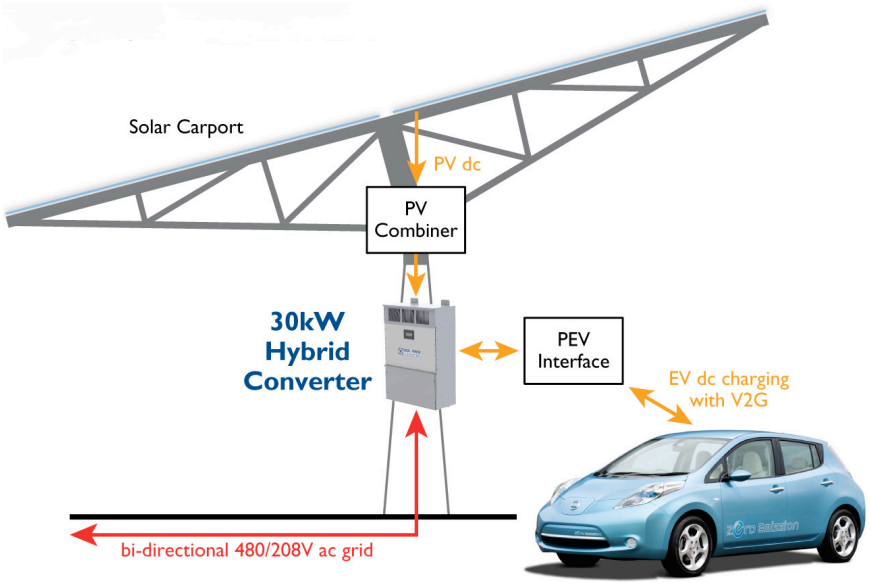

Figure 1. System level overview of IPC EVCS (from [3]).

The IPC AC link power converter has several design characteristics that separate it from others power converters currently on the market. It has been designed to be lightweight, with lower cost of system ownership and higher net system efficiencies as compared to an AC link converter of equal power [3]. Further investigations into the IPC AC link converter revealed that only limited information is known about the power capacitors used in this converter. Thus, these capacitors may be the weakest link in the overall system. This thesis will provide an in-depth exploration of this power capacitor's reliability.

C. EXPERIMENTAL APPROACH

Two testing phases were carried out in this work. Phase one was a characterization of the capacitors by measuring the leakage current versus voltage (IV) characteristics of each capacitor at various voltages. Phase two was a high voltage stress test (HVST), to evaluate capacitor lifetime, which is defined as the time at which the capacitor exhibits voltage breakdown. A more detailed description of these methodologies will be discussed in Chapter IV.

D. THESIS LAYOUT

This thesis is organized into six chapters. A basic introduction to capacitors and their properties is provided in Chapter II. Testing equipment is described in Chapter III. Description of the experimental layout and methodology used in this work is discussed in Chapter IV. Classification and lifetime reliability data are discussed and compared to established trends in Chapter V. Concluding remarks and possible future work are presented in Chapter VI.

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II. BACKGROUND

This first chapter presents information on capacitors needed to understand the characterization philosophy in describing thin film capacitors. This will allow for a better understanding of the reasons behind their use.

A. CAPACITOR

A capacitor is generally classified as a passive two-terminal element used to store energy electrostatically in an electric field [4]. The most common capacitor example is the parallel plate capacitor, which consists of two parallel plates separated by a narrow gap. Capacitance, C, can be affected by three separate parameters. These parameters are the permittivity of the material, ε, the area of the parallel plates of capacitor, A, and the plate separation between of the capacitor, d. Permittivity measures how well an electric field is affected by the dielectric medium [5] between the two plates of the capacitor. The relationship between these parameters can be quantified by

$$C = \frac{\varepsilon A}{d} \quad . \tag{1}$$

A visual representation of a typical parallel plate capacitor is presented in Figure 2.

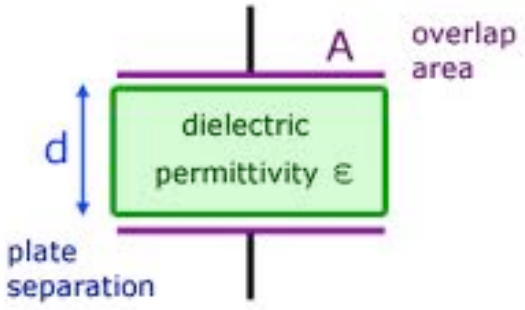

Figure 2. Parallel plate capacitor. From [4].

B. THIN FILM CAPACITOR

The parallel plate capacitor model is directly related to the physics of the thin film capacitor. Even though there are differences between a thin film capacitor and a generic parallel plate capacitor, the capacitance equation is still relevant. A general depiction of the thin film capacitor is illustrated below to identify the different layers in the capacitor.

Thin film capacitors use an insulating polymer film as the dielectric, sometimes combined with paper as an electrode carrier. The dielectric films, depending on the desired dielectric strength, are drawn in a special process to an extremely thin thickness. The electrodes of film capacitors may be metallized aluminum or zinc deposited upon the surface of the plastic film, or a separate metallic foil overlying the film. Two of these conductive layers are then wound into a cylinder shaped winding, usually flattened to reduce mounting space requirements on a printed circuit board, or layered as multiple single layers stacked together, to form a capacitor body [6].

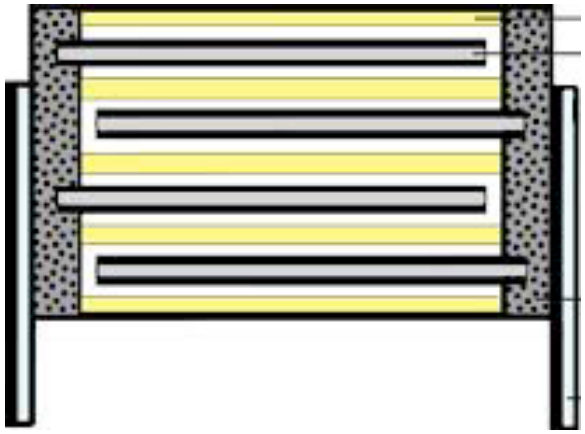

Figure 3. Thin Film Capacitor (from [5]).

A key advantage of modern film capacitor internal construction is direct contact to the electrodes on both ends of the winding. This contact keeps all current paths to the entire electrode very short. The setup behaves like a large number of individual capacitor elements connected in parallel, thus reducing the internal ohmic losses and the parasitic inductance. Various polymer film materials for the dielectric layer can be selected for desirable electrical characteristics, such as stability, wide temperature range, or ability to

withstand very high voltages. Polypropylene (PP) film capacitors are widely used because of their low electrical losses and their nearly linear behavior over a very wide frequency range, comparable only with ceramic capacitors. For simple high frequency filter circuits, polypropylene capacitors offer low-cost solutions with excellent long-term stability, allowing replacement of more expensive tantalum electrolytic capacitors. The film/foil variants of plastic film capacitors are especially capable of handling high to very high current surges [7].

C. SELF HEALING

One intrinsic characteristic that prolongs the reliability of PP film capacitors is self-healing [8]. This is an important feature for some applications, and is purely due to the manufacturing process of the thin film capacitor. Segmented material used in the electrodes of the thin film capacitor allows for the self-healing to take place, as illustrated below in Figure 4.

Figure 4. Segmented view of the thin film capacitor (from [8]).

When sufficient voltage is applied, any point defect in the dielectric film is short-circuited between the metallized electrodes. This short is then vaporized due to high arc temperature, since both the dielectric plastic material at the breakdown point and the metallized electrodes around the breakdown point are very thin (about 0.02 to 0.05 micrometers (μm)). The point-defect cause of the short circuit is burned out, and the resulting vapor pressure blows the arc away as well, up to the end of a segment. This process can complete in less than 10 microseconds (μs), often without interrupting the

useful operation of the afflicted capacitor [9]. The "pinholes" in the metallization caused by the self-healing arcs reduce the effective area of the capacitor, lowering the capacitance slightly. However, the magnitude of this reduction is quite low; even with several thousand defects burned out, this reduction usually is much smaller than 1% of the total capacitance of the capacitor [10].

Controlled self-healing provides a more predictable capacitor lifetime. With no controlled self-healing, the capacitance lifetime is limited by the avalanche effect, a sudden increase in the flow of an electrical current through a non-conducting or semiconducting solid when a sufficiently strong electrical field is applied [8]. This effect causes the capacitance to drop significantly due to the creation of shorts which do not clear, and leads to unpredictable failure of the component. The following figure illustrates the benefit of the self-healing characteristic when compared to capacitors with no self-healing characteristic based over a capacitor lifetime.

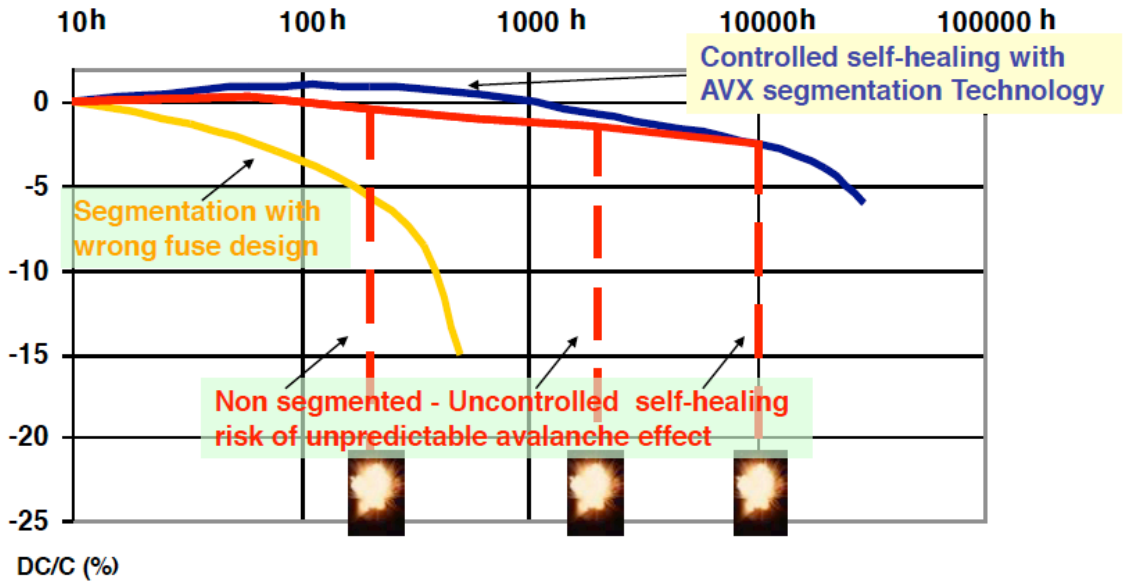

Figure 5. Lifetime comparison of controlled self-healing capacitors versus non-controlled self-healing capacitors (from [8]).

D. MODELING A THIN FILM CAPACITOR AS A SEMICONDUCTOR

Capacitors are generally only classified by their capacitance value. Further characterization is usually not performed. However, capacitor degradation can be accomplished by evaluating tertiary characteristics such as the frequency response of the capacitor impedance and the DC leakage current. The DC leakage current of any capacitor can be modeled by considering the dielectric to be a semiconductor. The polymer dielectric of a thin film capacitor can be viewed as a very wide bandgap semiconductor.

A semiconductor is an element that conducts more than an insulator but not quite as well as a conductor. In semiconductors, thermal energy is sufficient to cause a small number of electrons to escape from the valence bonds between the atoms (the valence band); these electrons transport instead into the higher-energy conduction band, in which they are relatively free. The resulting absences of electrons in the valence band are called holes [11]. The band diagram, illustrated in Figure 6, is used to visually identify the different bands and energy levels in the semiconductor model.

In band diagrams, the bandgap is represented by the energy difference (in electron volts) between the top of the valence band and the bottom of the conduction band in insulators and semiconductors. Substances with large band gaps are generally insulators, those with smaller band gaps are semiconductors, while conductors either have very small band gaps or none because the valence and conduction bands overlap [12].

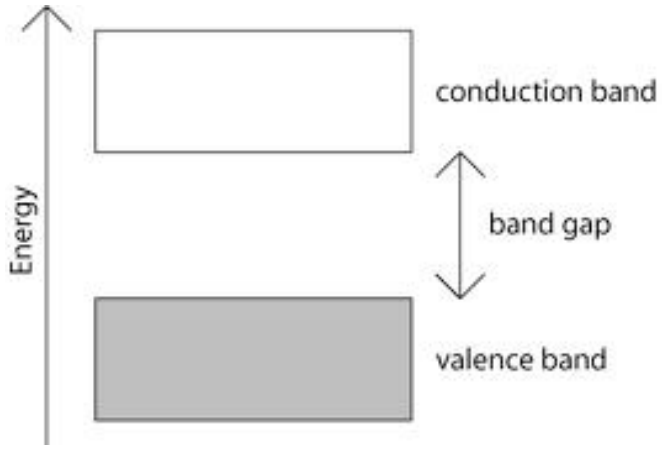

Figure 6. Generic band gap diagram of a semiconductor (from [11]).

For wide band gap materials the thermal energy available at room temperature excites very few electrons from the valance band into the conduction band; thus very few carriers exist inside the material and the material is therefore a poor conductor of current [13]. For silicon (Si), one of the most common materials used in semiconductors manufacturing, the band gap magnitude has a value of 1.12 electron volts (eV). For the thin film capacitor, the band gap magnitude of PP is 7.0 (eV) [14].

E. SPACE CHARGE LIMITED CURRENT

Space-Charge-Limited (SCL) emission is a well-known current mechanism that is often used to explain current conduction in insulating materials and wide bandgap semiconductors. Under an applied field, the free carrier concentration can be increased due to the injected carriers in the vicinity of the electrodes. When injected free-carrier concentration is larger than the thermal equilibrium value, the space charge effect is said to occur. The injected carriers influence the space charge and thus the electric field profile in the dielectric. The resulting field drives the current, which in turn influences the electric field. This current produced due to the presence of the space-charge effect is called space charged limited current [15].

Electron traps related to material defects also play a significant role in affecting SCL current injection. When a voltage is applied, the presence of energy levels within the forbidden band, called "traps," restrict the magnitude of the square law current-voltage characteristics of SCL. This effect is caused by the capture of electrons within the energy level. Trapping removes space charge from the semiconductor, delaying the onset of SCL. However, once enough charge has been injected to fill the trap levels, which occurs at a voltage V_{TFL}, SCL becomes the dominant current conduction mechanism in an insulator.

For a given material at a set energy level, there is a set concentration of traps within said material, N_t. The current-voltage characteristics can be observed for this material, depending on what the energy level is at the imbedded traps. Once all the traps are filled, the charge density of the excess carriers can be defined as

$$Q_{TFL} = qN_t d, \tag{2}$$

where q is defined as charge of an electron and d is defined as the distance between the electrodes. With slight manipulation from previous knowledge of the relationship between excess carrier charge density and the trap filled limit voltage, the following equation can be derived

$$V_{TFL} = {qN_t d}/{\varepsilon}. \quad (3)$$

This equation is used to describe the variation in the trapped filled voltage as the material properties are manipulated. Since the charge of the electron is constant, the only portion of equation (3) that will affect V_{TFL} will be the concentration of traps in the material, the distance between the plates of the capacitor or a change in permittivity of the capacitor material. For the purpose of this thesis, direct comparison of the V_{TFL} values will be used since neither the distance between the plates of the capacitor or the dielectric constant is quantified.

A representative set of IV characteristics in a capacitor is shown in Figure 7. At relatively low voltages, the voltage current trace follows Ohm's law. This is mainly due to the thermal equilibrium free-carriers that exist in the material. As the voltage continues to increases, the SCL current begins to affect the IV relationship characteristic. However, the SCL current is suppressed due to electrons beginning to become trapped in what is called the Shallow Trapping Field Region. As the voltage continues to increase, the SCL current effect continues to rise as more electrons become trapped until all the trapped states in the semiconductor material become filled. Once all the trapped states are filled, the voltage is said to be at V_{TFL}. This limit is indicated by the current-voltage trace showing a vertical jump in current. Once V_{TFL} has been reached, the IV characteristic shifts to the trap-free square law relationship, since all the traps in the material are now filled. By knowing the current values before and after reaching V_{TFL}, the concentration of the trapped states can be calculated [16].

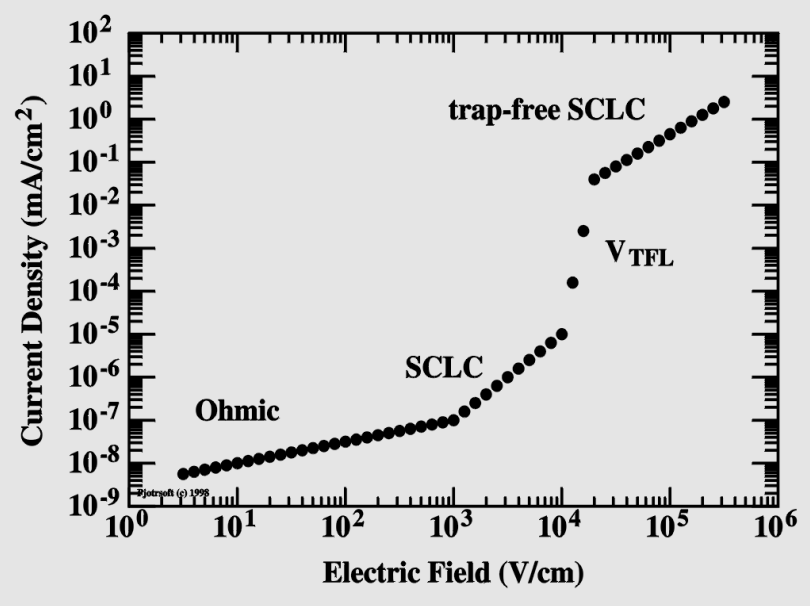

Figure 7. Log-log plot of current density versus electric field to showcase the change in the current-voltage relationship due to a material with electron injection traps (from [16]).

F. HIGH VOLTAGE CONSIDERATIONS

Safety is always paramount when dealing with high voltages. The National Electrical Code (NEC) defines high voltage as any voltage over 600 V [17]. To prevent any damage to equipment or to personnel, safety precautions must to be taken throughout the testing. One of the most important aspects of safety is situational awareness. A safety procedure was developed to prevent any damage to personnel or equipment. As long as the safety procedure is adhered to, the possibility to cause damage is minimized. The safety procedure that was utilized is included in Appendix A.

The equipment used for this thesis also has safety features. The high voltage power supply (HVPS) has limits associated with it to prevent causing damage to the user or equipment. The HVPS has multiple safety switches that must be actuated prior to power being supplied to the circuit board. The circuit board itself is placed in a metal holder, which is then placed inside of a laboratory oven. The laboratory oven prevents the user from touching the circuit board when voltage is applied. When these precautions

and testing procedure are used, the ability to cause damage to equipment or personnel is minimized.

This chapter discussed the background fundamentals necessary to perform the investigation into thin film characterization and lifetime component reliability. Chapter III will discuss the equipment utilized for this investigation and how they were used.

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III. TESTING EQUIPMENT UTILIZED

A variety of equipment was required to perform the two described tests. This chapter will highlight the equipment used so an accurate duplication of this work is available for future studies.

A. HIGH VOLTAGE POWER SUPPLY EQUIPMENT

The capacitors tested have a high voltage rating of 1500 VDC. In order to properly characterize and perform a reliability test on these capacitors, a high voltage power supply was procured. The Stanford Research Systems Series PS300 High Voltage Power Supply was determined to be the best power supply for the required testing. The specifications data sheet for this equipment is included in Appendix B for further information.

B. LOW NOISE PRE-AMPLIFIER

Typical capacitor leakage current has very low amplitude signal strength associated with the measurements, on the order of picoamps (pA). For most equipment, measuring such a small signal is difficult because of poor accuracy. To mitigate this problem, the use of an amplification circuit is required to increase the signal to a level in which the measurement equipment can accurately detect the signal. A low noise amplifier, the Stanford Research Systems Low-Noise Preamplifier Model SR560, was used to amplify voltage signals across a sensing resistor to detectable level. The SR560 was specifically chosen due to the built in dual pole filtering in the amplifier. The specifications data sheet for this equipment is included in Appendix B.

C. TESTING LABRATORY OVEN

For the lifetime reliability testing, the capacitor was stressed at a higher temperature to expedite the failure of the component. The testing oven was able to keep the test circuit at a constant 70 degrees Celsius for the duration of the test.

Additionally, since the signal level that was measured was so small, a shielding mechanism was needed to minimize the external noise. It was determined that the extra equipment running in the laboratory was the cause of this external noise. This added unwanted fluctuations in the low level signal being measured, making any data collection taken less than optimal. The solution to minimize this noise was to place the test circuit board into a metal box, or shielded environment, in which the external noises would be minimized. This added shielding minimized some of the noise issues, allowing for a more accurate signal measurement.

D. FLUKE PRECISION MULTIMETER

Accurate measurements are imperative during the collection of the data for this thesis. A multimeter with a GPIB was required with the use of a computer-based data collection method, which is described in depth in the next section of this thesis. The Fluke 8846A Precision Multimeter, with 6.5 digits of precision, was used to detect the low level signals encountered in current sensing measurements.

E. LABORATORY VIRTUAL INSTRUMENT ENGINEERING WORKBENCH (LABVIEW)

For this thesis, a computer-based simulation program, LabVIEW, was written to collect and record capacitor data during each phase of testing. The program was designed to allow for the testing of two capacitors on one circuit board simultaneously. Since only two low noise pre-amplifiers were on hand, only two capacitors could be tested and recorded at one time. A detailed description of the software and its functionality will be discussed in Chapter IV.

F. CABLES AND CONNECTORS

Three separate types of cables were needed for the film capacitor testing; a Bayonet Neill Concelman (BNC) cables, HVPS cable and GPIB cable. Each of these cables will be discussed in detail as to why they were used and the capacity in which they have been used. Figure 8 illustrates how each cable has been utilized for the characterization and reliability testing.

1. BNC Cable

For the majority of test equipment connections, a BNC cable was used. The word bayonet refers to the connector's style and Paul Neill and Carl Concelman were the Bell Labs engineers who developed it. BNC connectors can be used well into the microwave range and can tolerate as much as 500V [18]. BNC cables also have a locking mechanism on each end that must be turned 45 degrees when removing or installing the cable. This prevents the cable from inadvertently being disconnected while a test is in progress.

For the application used for this thesis, the order of magnitude of voltage seen by each cable is much smaller. Due to the sheer number of BNC cables available and the ease of use with the test equipment available, BNC cables were determined to be the best cable available for this testing.

2. HVPS Cable

The HVPS cable is a specialized coaxial cable that utilizes a high voltage bayonet connector. The cable itself has a voltage rating in excess of 5000V DC. The HVPS cable also has a locking mechanism on each end that must be turned 45 degrees when removing or installing the cable. This prevents the cable from inadvertently being disconnected while testing is in progress. Since this cable is made for high voltage applications, the connectors associated with the HVPS are of the same type and design. The HVPS cable connected the HVPS to the testing circuit board.

3. GPIB Cable

The GPIB cable serves the purpose of providing a communication link between the Fluke Precision multimeters and the LabVIEW program. The GPIB cable can be connected to a variety of different equipment from different manufacturers. It provides the communication network structure for the data requested by the LabVIEW program to be collected from the measurement devices, such as the Fluke Precision multimeter. This minimizes the need for an operator to input the required conditions to run the experiment and then record the experienced results.

G. SYSTEM LEVEL OVERVIEW

The overall system used for the characterization and reliability testing was designed to maximize the number of devices that can be tested simultaneously and simplify the data taking process. The system level overview illustrated in Figure 8, includes the supporting equipment used and the method of connecting all equipment together for testing.

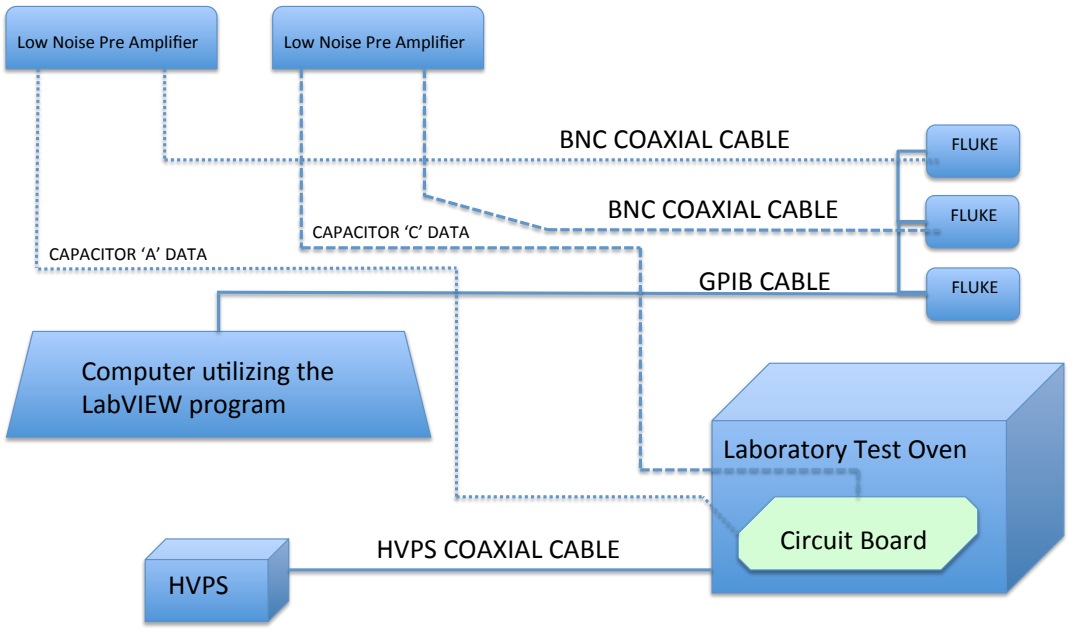

Figure 8. Overview of Equipment and Cable Layout

This chapter discussed the equipment collected and used for the investigation into the characterization and lifetime reliability of the thin film capacitor. Chapter IV will highlight the experimental circuit layout and the methodology used for this investigation.

IV. EXPERIMENTAL CIRCUIT LAYOUT AND METHODOLOGY

This chapter will highlight the experimental circuit that was developed and used for the investigation into the thin film capacitor. The methodology used for both the characterization and lifetime reliability testing will also be discussed.

A. CIRCUIT OPTIMIZATION

Noise is a constant problem within any electronic system, specifically when trying to measure extremely small signals. It causes a disturbance in the datum set and limits the ability to distinguish what the actual component value being measured is. In the thin film capacitors, the noise can be categorized as Johnson-Nyquist, otherwise known as thermal, noise. Thermal noise is electronic noise generated by the thermal agitation of the charge carriers, usually electrons, inside an electrical conductor at equilibrium, which happens regardless of any applied voltage. Additionally, noise due to radio frequency (RF) on power line sources can be inductively coupled to the test circuit, drowning out low-level signals.

Since thermal and RF noise are unwanted factors the testing process conducted in this thesis must be approached in a slightly different manner. Due to the relatively small signal that is being measured while testing these thin film capacitors, the signal must be amplified and then filtered. The amplification of the measured signal coupled with the use of a filter removes the thermal noise. These added steps make characterizing the thin film capacitor more difficult, but the end result is a more accurate final measurement.

B. CIRCUIT LAYOUT, DESIGN, AND SUPPORTING EQUIPMENT

In order to expedite the testing of the capacitors for characterization and for the HVST, a testing circuit board was developed.

1. Printed Circuit Board (PCB) Design

A PCB was designed to facilitate the rapid testing of multiple capacitors at one time. The circuit board allows for testing multiple capacitors simultaneously while minimizing the number of wires required.

a. Circuit Board Design

The circuit board designed contains two planes, a high voltage plane and a ground plane. For this testing, the ground plane was placed on the top and the high voltage plane was placed on the bottom. The design choice was taken to ensure that it would be difficult for personnel conducting the experiment to touch the high voltage plane.

Due to expected applied voltages greater than 4000 V, significant design considerations were required to prevent damage to the testing equipment, the capacitors, or the board itself during testing. Two parameters that needed to be verified during the design were creepage and clearance. Creepage distance is the leakage path along the surface of the PCB from one trace to another [19]. Clearance distance is the space required between two parts that if touched could cause significant damage. These distances must be maximized in order to minimize the leakage currents that can exist on the board between areas of high and low potential. This was accomplished by rounding all the corners of the HVP as they reached the edge of the circuit board and when any shape was constructed on the ground plane. The circuit boards material was also verified to be able to withstand the voltage that was expected for this testing. Figure 9 illustrates these design parameters.

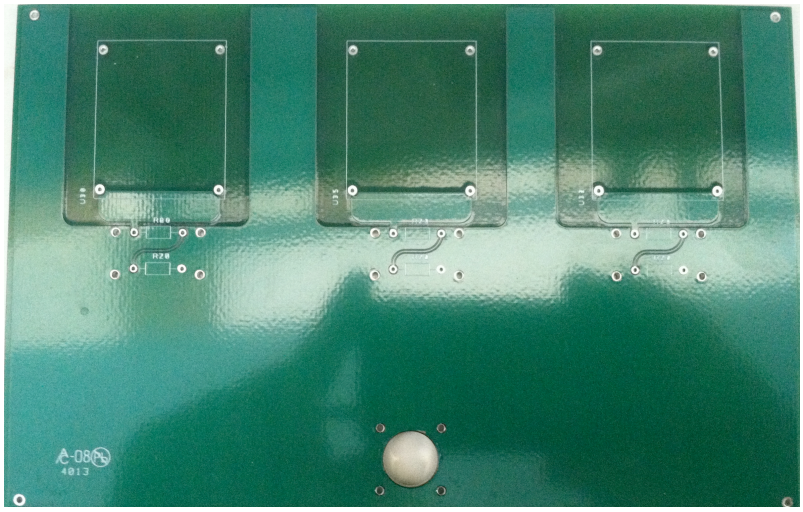

Figure 9. New Circuit Board.

b. Circuit Layout

The circuit board was designed to expedite testing by having multiple capacitors placed on the board. Each board was numbered from one to eight. Each capacitor was labeled A, B, or C on each board. This allowed for easy identification of the capacitor while conducting the tests. Figure 10 depicts the circuit board ready for testing the capacitors.

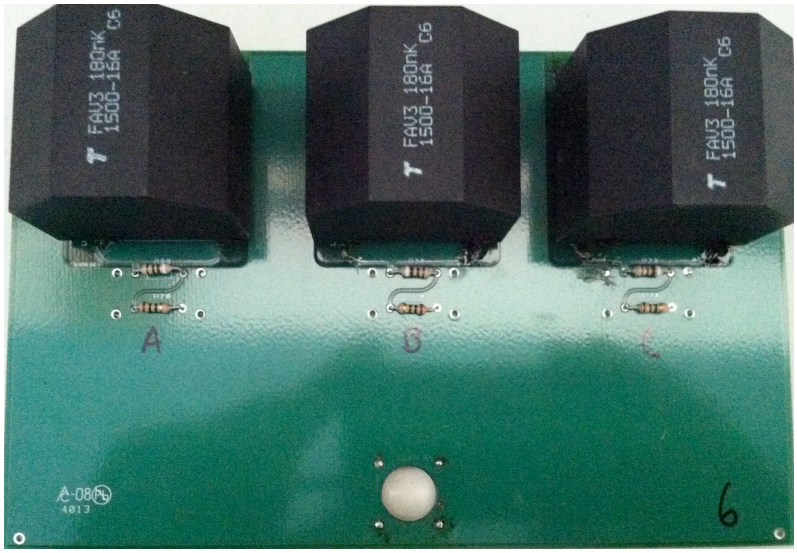

Figure 10. Circuit board layout with components installed.

Each capacitor utilized a noise-dampening set of resistors. Table 1 shows exactly what resistor values were used for each board and for each capacitor associated with that circuit board.

Table 1. Resistor values for each capacitor used for characterization and reliability testing. Board numbers eight and nine were used with the copper-clad box.

Board Number	Capacitor A		Capacitor B		Capacitor C	
1	9.110	1.043	9.080	1.001	9.130	0.999
2	9.000	1.009	9.040	1.005	9.130	0.997
3	9.210	1.006	9.020	1.005	9.130	0.999
4	9.200	1.002	9.070	1.009	9.260	1.006
5	9.030	1.004	9.070	1.009	9.260	1.006
6	9.220	1.010	9.180	1.001	9.110	1.010
7	9.200	0.999	9.070	1.009	9.100	1.003
8	116 KΩ					
9	116 KΩ					
Note: All units are in mega ohms of resistance (MΩ) unless otherwise noted.						

A special bracket was created to form a 90-degree angle from the circuit board to allow the HVPS fitting to be soldered to the HVP of the circuit board. This special bracket will be referred to as the HVPS connector bracket for the remainder of this thesis. With the exception of the HVPS connector bracket, all components on the circuit board were surfaced mounted and soldered in place. Any exposed wires or soldering joint was wrapped with high voltage tape to prevent any unwanted events from occurring. Any area that could not be protected with high voltage tape was coated with Super Corona Dope, a liquid insulation product for high voltage applications. The HVPS equipment will be described further in Chapter IV.

c. Circuit Supporting Equipment

The circuit board was designed to have the HVP on the bottom of it, so a circuit board holder had to be developed to keep the board elevated off the deck at all times. The design that was created allows the circuit board to be installed after first installing

the HVPS connector bracket. The circuit board holder utilized carbon steel metal and allows for easy installation and removal of a circuit board for testing. The holder was then attached to a wooden base structure, designed to allow the necessary testing cable to be run underneath it in a cableway. Using this cableway in conjunction with holes cut in the board surface, the testing cables were passed underneath the wooden base structure and connected to the circuit board. The following figure depicts the wooden base structure and the circuit board holder.

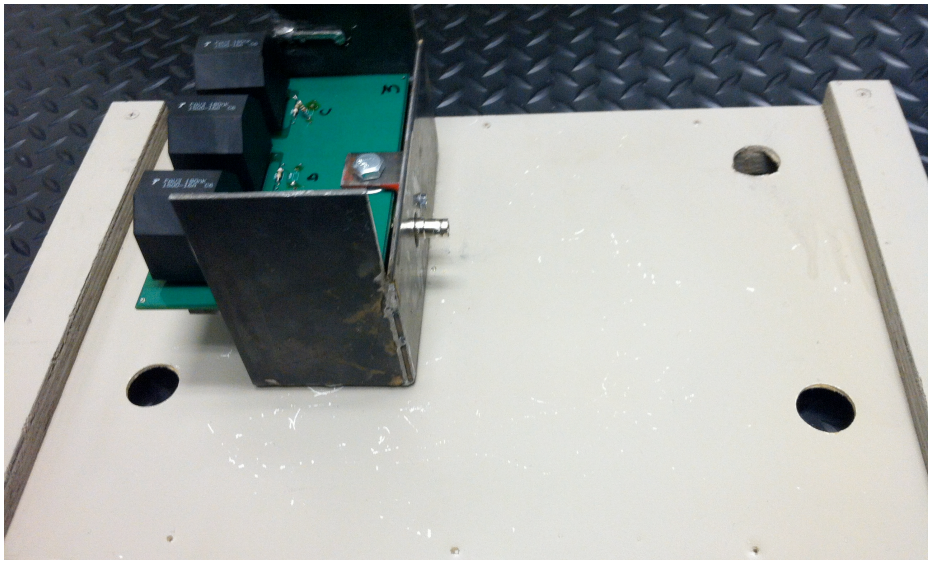

Figure 11. Circuit board holder and wooden base structure.

In order to prep a PCB for characterization testing, first we bolt the HVPD connector bracket to the circuit board. Once connected, the HVPS connector is soldered to the HVP on the PCB board. Once complete, the exposed wires must be wrapped with high voltage electrical tape. The PCB is the inserted into the circuit board holder. Using the supplied self-tapping screw, the circuit board holder is attached to the HVPS connector bracket. This system is designed to prevent the circuit board from undesired movement when attaching leads, the high voltage power supply cable, or adjusting the circuit board prior to testing. Finally, the wooden base is placed in the testing oven and all required leads are attached to the circuit so testing can begin.

2. Copper Box Test Circuit Design

An additional testing circuit board design was utilized in order to minimize the noise associated with the low-level current leakage measurements. One method to minimize noise is to create a shielded copper structure out of insulated copper wafer boards. These boards are very robust in nature and are very useful in test circuits. Using this fully enclosed copper-clad box allowed for minimized background noise during testing. Additionally, the direct connections for the circuit elements reduce spurious leakage currents, which may invalidate measurements [20].

The direct connection method does not use the traditional method of soldering the electrical components on to a circuit board. Instead, the components are connected to each other via soldered wire connections. The direct connection method is fairly common, specifically when used with a copper clad board. Capacitor numbers eight and nine were used in the copper-clad box during the characterization testing. The following figure illustrates the way the copper clad box was constructed and the way the air connection method was utilized for noise minimization.

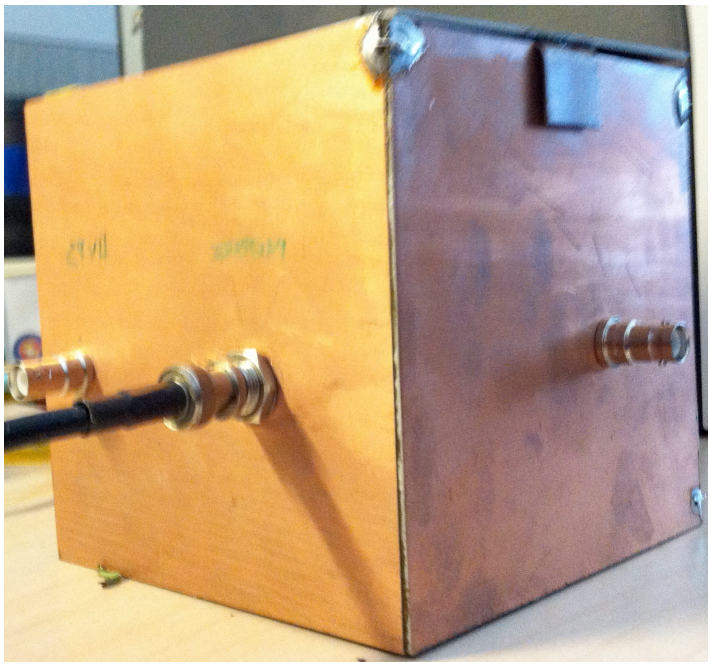

Figure 12. Copper box utilized to prevent excessive noise and signal distortion.

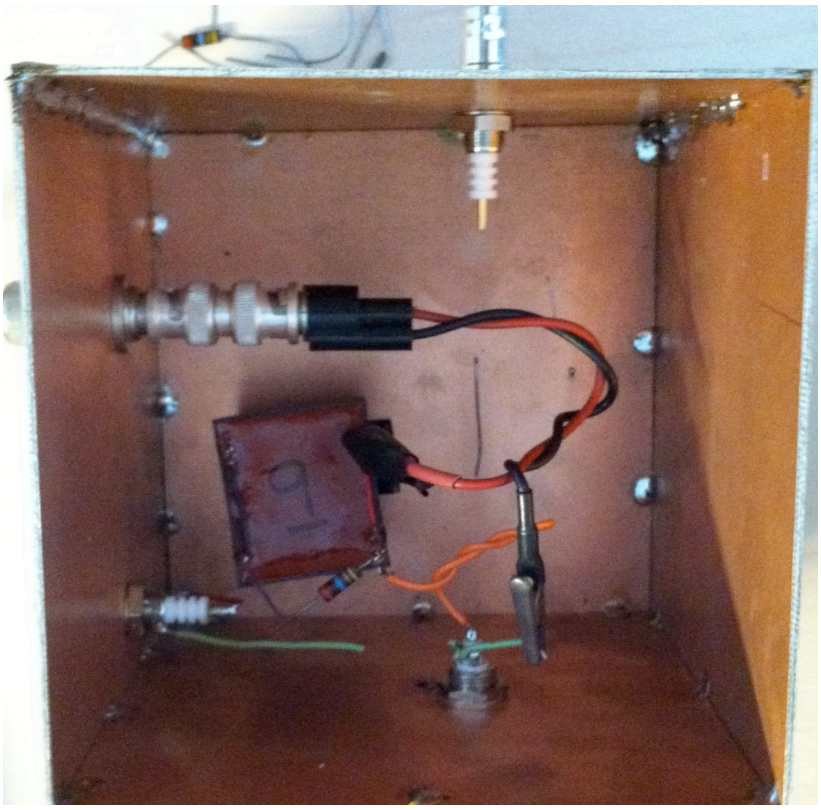

Figure 13. Air connection method used to prevent excessive noise and signal distortion.

The testing setup used for the characterization incorporating the copper-clad box is more simplistic as compared to the initial characterization testing method. The data measurements were collected with the use of one low noise preamplifier and one Fluke 8846A precision multimeter. Since only one capacitor could be tested in the copper-clad box at a time, the excessive Fluke 8846A precision multimeters and low noise preamplifier were removed from the testing system. The data was still collected via a GPIB cable and recorded with the use of the same LabVIEW program that was utilized for the characterization with the PCB test circuit board. The copper-clad box system overview is illustrated in Figure 14.

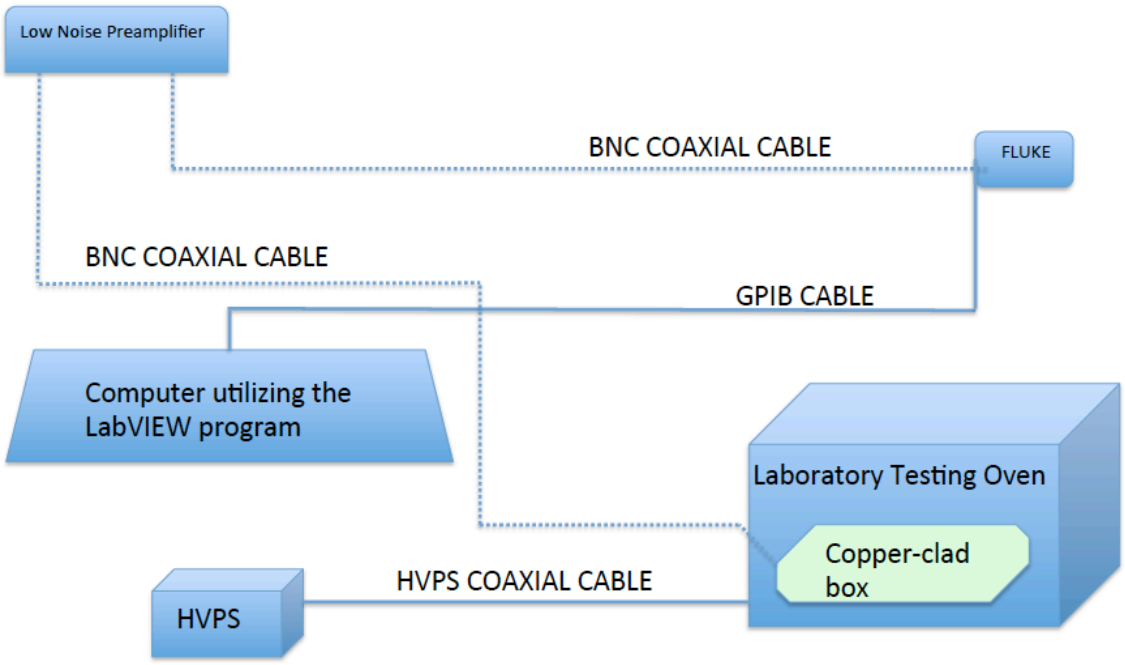

Figure 14. Characterization system overview with the use of the copper-clad box and air connected components.

C. METHODOLOGY

The experimental data collection for this thesis was performed in two phases. Two separate tests were performed, utilizing the same circuit boards to minimize time between experiments. The initial phase was to complete a characterization datum set of the thin film capacitors. Characterization was performed similar to what would be done to characterize a semiconductor. The underlying DC leakage current measurements were discussed in Chapter II. The second phase of testing was designed to provide insight into the expected lifetime reliability of these capacitors.

1. LabVIEW Utilization for Data Retrieval

In order to calculate and present the data in a useful method, a reliable method of measuring the leakage current was designed with the use of a LabVIEW program. Since the current values are so small and noise is prevalent in the laboratory environment, the leakage current was calculated by measuring the voltage across a known value resistor.

The use of this program allowed for the circuit to be under test for a substantial amount of time without the need for human interaction until the test was complete. An additional advantage of the LabVIEW program was the ability to measure up to three separate capacitors simultaneously. Measuring the voltage itself was accomplished through the use of the Fluke 8846A digital multimeter.

The program utilized user inputs in order to alter the five user-defined input parameters that must be established prior to the test starting. These inputs were: applied test voltage, number of testing iterations, testing duration (in seconds), test points averaging, and the testing temperature. The characterization and reliability tests required different user inputs, and will be described later in this chapter.

2. Characterization Methodology

After researching several different methods in which to accurately measure the leakage current of the thin film capacitor, it was determined that the most accurate method available would be to determine the leakage current by measuring the voltage drop across the resistor in series with the thin film capacitor. Using the standard form of Ohms law,

$$V_{MEAS} = I_{LEAK} R \tag{4}$$

where V is the measured voltage across the resistor in volts (V), R is the resistor value in Ohms (Ω) and I is the leakage current in Amps (A), the equation can be rearranging to solve for the leakage current, which becomes

$$I_{LEAK} = {V_{MEAS}}/{R} \ . \tag{5}$$

The resistor values used for this testing were discussed earlier in this chapter, and are listed in Table 1. Each circuit board tested followed this principle of measuring leakage current. Test circuit boards one through seven were used with the characterization testing with the traditional test setup depicted in Figure 8. Capacitor numbers eight and nine were used in the copper-clad box during the characterization testing. This method of calculating leakage current was performed predominantly in the

LabVIEW program as to minimize any possible calculation errors and to streamline the process due to the large amount of individual measurements taken during any given test.

a. Characterization Testing Parameters

For the characterization testing, the applied test voltage was measured from 0V to 500V DC, in incremental steps of 50V DC. Every two seconds, the voltage across the resistor was measured and then recorded. Each step of voltage was tested for a testing duration of 2000 seconds and an average value was calculated over the last 100 data points taken. All characterization testing was accomplished at room temperature, 25 degrees Celsius. The data was averaged to get for an accurate value of the voltage measured, using a standard averaging formula of

$$V_{AVG} = \frac{\sum_{k=1}^{n} V_k}{n} \tag{6}$$

where n is the set number of data points the average is taken over, V_k is the measured voltage across the resistor at measurement k, and V_{AVG} is the average measured voltage. Each test was run once and then another test circuit board was installed to perform the characterization testing again. The characterization of the PCB test boards was conducted first, followed by characterization with the copper-clad box with the air-connected components. Results obtained from the characterization testing can be found in Chapter V.

3. HVST Methodology

The high voltage stress test required the capacitors to be stressed for a long time period until a significant change was seen in the capacitance value of the capacitor. Generally, a negative drop in the capacitance value of two to five percent predicts a capacitor that is degrading enough to require the capacitor to be replaced. Nominally, to accomplish this type of testing the capacitor would be tested at rated voltage for the expected lifetime. Due to time constraints, it was not feasible to test the capacitors at rated voltage for 100000 hours to determine whether they would fail. Instead, device failure was accelerated with the use of excessive stress.

The two main methods of capacitor degradation acceleration are due to excessively high voltage and higher than designed for ambient temperatures. By exposing the capacitors to higher voltages and higher temperature simultaneously, the capacitors should degrade much faster. The main method of determining the breakdown will be the change in capacitance value. As time permits the capacitors will be stressed in the laboratory simulation. If insufficient data exists to determine the lifetime of the capacitor at the tested voltage, the lifetime will have to be extrapolated. Extrapolated lifetime data is not as accurate as the continued lifetime testing data, but it gives the expected lifetime of the capacitor under similar operating conditions. The extrapolation method will be presented with the reliability testing results in Chapter V. The manufacturer has performed similar reliability testing on these capacitors, and are enclosed in Appendix B of this thesis.

a. Constant Voltage Stress Test

In order to perform the constant voltage stress testing in a time efficient manner, the capacitor will be tested over a seven-day period. The applied voltage was set successively to 1000V DC, 2000V DC and 2500V DC. Each test was run for a 24-hour period with the testing oven set to a constant elevated temperature of 70 degrees Celsius. After each 24-hour period, the capacitance value was measured. This test was used to identify any significant changes in the capacitance value. Three measurements of the capacitance value were taken and averaged for a more accurate value using Equation (6). Once the capacitance values were recorded, the circuit was reconnected in the testing oven and then stress testing resumed until all data was recorded.

These capacitance values were then plotted as a function of time to showcase their change in capacitance over the lifetime of the stress test. These results are discussed in Chapter V.

The methodology and designed experimental circuit layout was discussed in this chapter. Next, the results of this experimental layout are analyzed and discussed in Chapter V.

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V. DATA RESULTS AND ANALYSIS

Characterization and reliability data will be presented and discussed in this chapter. The reliability data will also be compared to the provided manufactures data sheet to provide insight into the lifetime that can be expected from these thin film capacitors.

A. CHARACTERIZATION DATA

Characterization testing was performed on each PCB circuit board and was also performed twice with the copper-clad box using the air connected component method. Characterization data was placed on a plot to showcase the SCL current and PF effect during the testing. In order to plot the characterization data, simple calculations had to be performed in order to translate the measured amplified voltage data into usable current data for analysis. At the time the data is placed in the worksheet document by the LabVIEW program, the leakage current has been calculated and averaged, using methods described in Chapter IV.

Initially, the data recorded a value for the leakage current when no voltage had been applied to the capacitor under test. This value had to be subtracted out from the leakage current measured at each voltage step in order to find the actual measured leakage current. Using the equation

$$Zero\ I = abs[I(n) - I(0)] \tag{7}$$

the leakage current recorded for the no-voltage condition was subtracted from the leakage current readings to zero the data out. This allowed all measurements taken to start from a zero current value so a common comparison could be made for all IV curves. The power law and square law relationships also could be developed from starting from a zeroed current level.

1. Results from PCB Circuit Rest Board

Recorded values and calculated zeroed current developed using equation (7) from test circuit board nine, capacitor A are displayed in Table 2.

Table 2. Measured parameters and calculations performed to characterize the thin film capacitor. Data shown is taken from test board number nine, capacitor A.

Test Voltage (V)	R Measured (Ω)	I Measured (A)	Zeroed I (A)
0	1.002670E+05	-2.216882E-09	0
50	1.002670E+05	-2.155067E-09	6.181500E-11
100	1.002670E+05	-2.155815E-09	6.106700E-11
150	1.002670E+05	-2.050586E-09	1.662960E-10
200	1.002670E+05	-2.095426E-09	1.214560E-10
250	1.002670E+05	-2.096633E-09	1.202490E-10
300	1.002670E+05	-2.057847E-09	1.590350E-10
350	1.002670E+05	-2.108302E-09	1.085800E-10
400	1.002670E+05	2.186184E-09	4.403066E-09
450	1.002670E+05	2.237506E-09	4.454388E-09
500	1.002670E+05	2.356887E-09	4.573769E-09

Using the data presented in Table 2, a log-log IV plot was constructed using the applied voltage and the zero averaged current.

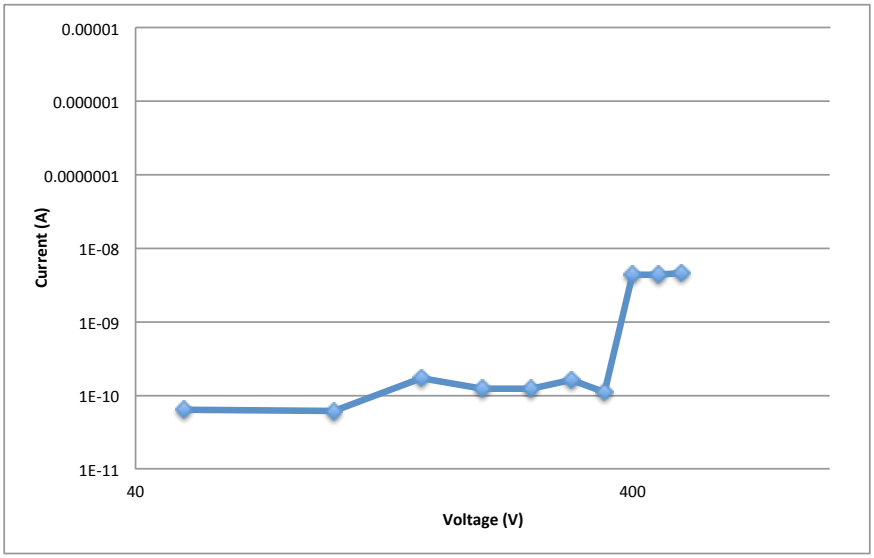

Figure 15. Log-log plot of zeroed current versus test voltage from PCB circuit board and copper-clad box depicting the change in current as voltage is incrementally increased for capacitor A, circuit board 9.

The IV plot shown in Figure 15 was then compared to that presented in Figure 7. Our results indicate a rise in voltage potential between 350V DC and 400V DC in Figure 15, which corresponds to that observed in Figure 7.

This IV plot depicts an excellent example of trap filled SCLC, and the step rise in current at V_{TFL} is easily visible. For this particular test circuit the rise in current starts at 350V DC. Once the current jump has taken place, the power law relationship between current and voltage is said to be 'trap free'. The voltage trap filled limit, V_{TFL} is reached, which for this capacitor was estimated to be 400V DC. The "trap free" Ohmic relationship between current and voltage is reached due to all the material defect traps being filled, and the free carrier concentration is effectively zero.

2. Results from Copper-clad Box with Air Connection Method

The recorded values and calculated zeroed current developed using Equation (5) from the copper-clad box with air-connected components are displayed in Table 3.

Table 3. Measured parameters and calculations performed to characterize the thin film capacitor. Data shown is taken from the copper-clad box with air connection method and capacitor nine.

Test Voltage (V)	I Measured (A)	R Measured (Ω)	Zeroed I (A)
0	1.3351E-07	9.9643E+04	0
50	3.9491E-08	9.9643E+04	9.40195E-08
100	-1.4633E-08	9.9643E+04	1.48144E-07
150	-3.2293E-08	9.9643E+04	1.65804E-07
200	-4.6624E-08	9.9643E+04	1.80135E-07
250	-6.0815E-08	9.9643E+04	1.94325E-07
300	-8.0513E-07	9.9643E+04	9.38642E-07
350	-1.0313E-06	9.9643E+04	1.16477E-06
400	-2.0997E-07	9.9643E+04	1.43483E-06
450	-1.9871E-08	9.9643E+04	1.53382E-06
500	-1.0319E-06	9.9643E+04	1.65403E-06

Using the data presented in Table 3, a log-log IV plot was constructed using the applied voltage and the zero averaged current.

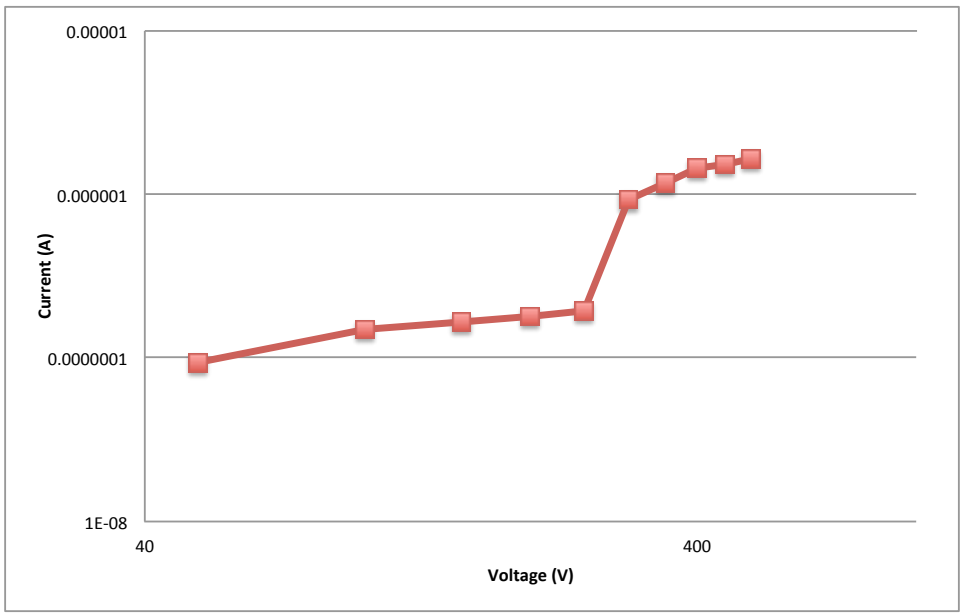

Figure 16. Log-log plot of zeroed current versus test voltage from PCB circuit board and copper-clad box depicting the change in current as voltage is incrementally increased on capacitor 9.

The IV plot shown in Figure 16 was then compared to that shown in Figure 7. When compared, the rise in voltage potential between 250V DC and 300V DC shown in Figure 15 can be attributed to the existence of SCLC in this capacitor.

The rise in current at 250V DC can be said to occur due to SCLC, specifically since the measured current before the jump step in current followed the power law relationship. At 300V DC, V_{TFL} is reached for this capacitor.

3. Comparison of the Two Test Circuit Designs

Through the data collection phase, circuit designs changed to assist in the minimization of the noise seen by the measurement equipment. The copper-clad box with the air connected components exhibited a much more accurate display of SCLC and V_{TFL} when compared to Figure 15.

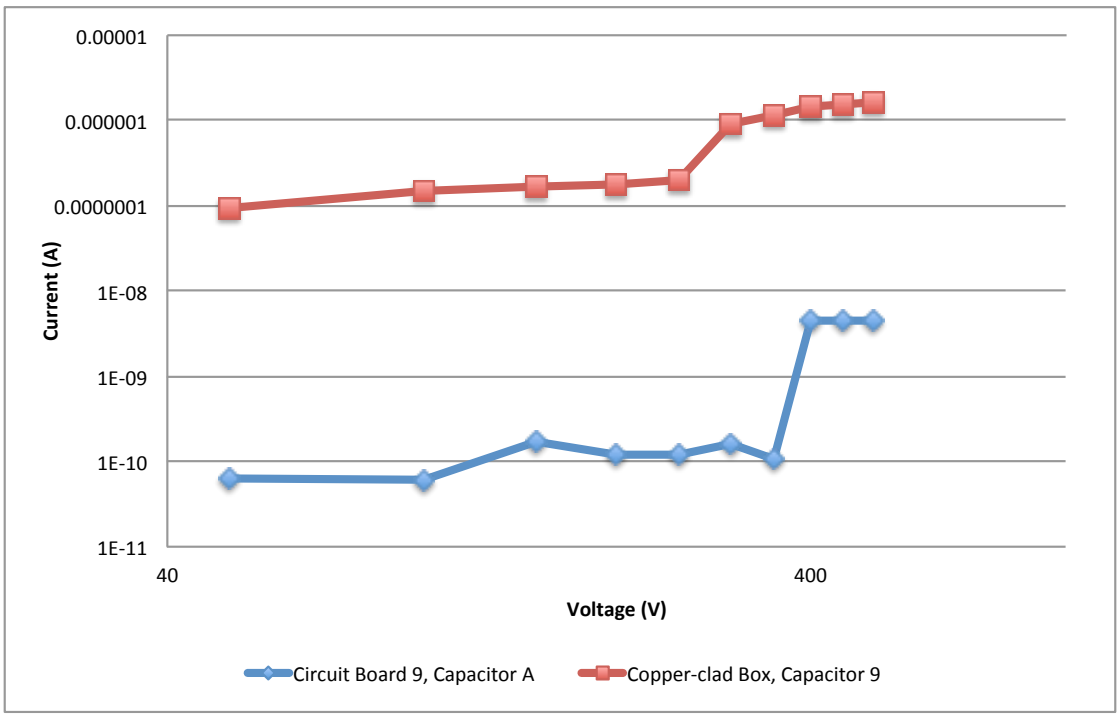

Figure 17. Log-log IV plot of zeroed current versus test voltage from the copper-clad box with air connection method and the PCB test circuit board

The main differences between the PCB circuit and the copper-clad box are illustrated in Figure 17. One specific point of interest is the alteration in the power law relationship between the copper-clad box method and the PCB circuit method. The second point of interest in comparing these to IV plots is the point in which the SCL emission starts to present itself.

The overall trend is that of a power law relationship between the current and voltage, which is what is expected. Fluctuations in the power law in the PCB circuit board are due to the excessive noise that was present in the laboratory-testing environment. The rise in current for the copper-clad box is due to a change in the low pre-noise amplifier, which was recalibrated prior to the copper-clad box testing. It can also be seen that the use of the copper-clad box and air connection method can minimize the external noise, specifically when using a recalibrated amplification measurement circuit.

4. Initial Circuit Design Characterization Data

Due to the excessive background noise levels associated with some of the PCB circuit boards, only data from two of the test boards were usable for analysis. The usability of the test data was determined by the repeatability of the datum set. If the datum could not be reproduced with limited variation in the leakage current at each voltage step, the datum set was determined to contain excessive noise. These data sets were then removed since they would not properly allow for the characterization of the thin film capacitors.

The data collected that was deemed useless is presented and discussed in this portion of the thesis since the data was taken and analyzed. This data highlights the issues associated with excessive noise issues that were prevalent during the characterization testing. The noise issues were also different with every test that was conducted. This noise contribution was minimized in the data displayed in Figure 15 and Figure 16 by adding in the precision multimeters and low noise preamplifier set to a substantial gain to raise the low leakage current measurement above the noise threshold. The IV plots of these data sets are provided in Figure 18 to illustrate the difficulties involved in repeating measurements when no precautions were taken to minimize noise impacts.

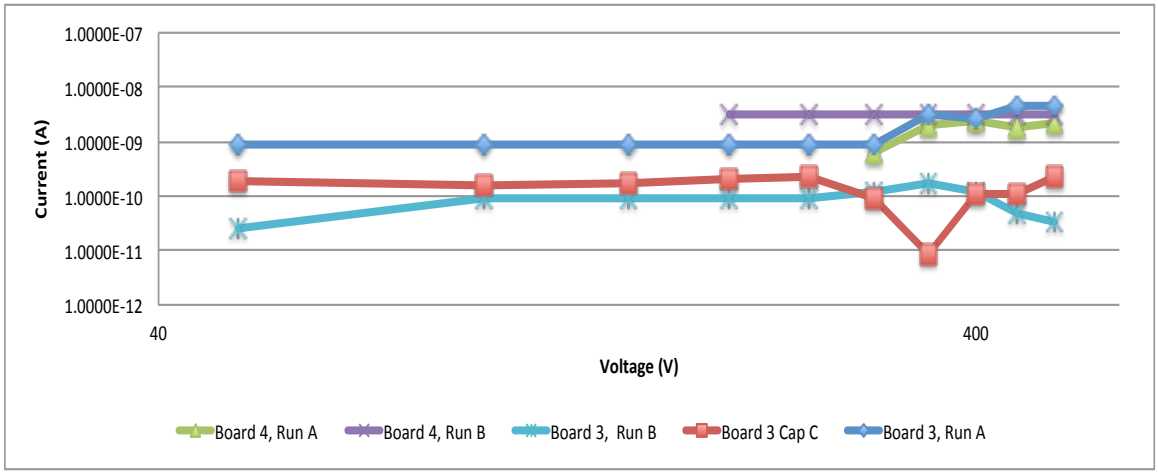

Figure 18. Log-log IV plot of zeroed current versus test voltage from the PCB circuit boards which shows the excessive signal distortion due to thermal noise present during characterization testing.

When the IV data from Figure 17 are compared to that shown in Figure 18, it is easily seen that the data are distorted by noise. This data were also not repeatable, although multiple iterations were performed to verify this before flagging these data sets as distorted. All testing was performed in the same test environment, so each datum set was exposed to the same type of background noise. This data also show how well the copper-clad box and air connected component method works at minimizing signal distorting noise when compared to the PCB circuit.

B. LIFETIME RELIABILITY DATA

Lifetime reliability testing was performed on one PCB circuit board. The recorded capacitance values at each time interval at each test voltages are shown in Table 4.

Table 4. Recorded data during the lifetime reliability testing. All stress voltages were applied over a 48-hour period. The 2500 VDC test voltage was applied over a 96-hour due to an observation of an upshift in capacitance value during the testing.

Run Index	Test Voltage (V)	Time (Hours)	Capacitance Value (F)			AVG Capacitance (F)
1	1000	0	1.8180E-10	1.8380E-10	1.8380E-10	1.8313E-10
2	1000	24	1.8223E-10	1.8232E-10	1.8234E-10	1.8230E-10
3	1000	48	1.8115E-10	1.8129E-10	1.8132E-10	1.8125E-10
4	2000	0	1.8180E-10	1.8380E-10	1.8380E-10	1.8313E-10
5	2000	24	1.8268E-10	1.8270E-10	1.8271E-10	1.8269E-10
6	2000	48	1.8124E-10	1.8130E-10	1.8133E-10	1.8129E-10
7	2500	0	1.8363E-10	1.8363E-10	1.8363E-10	1.8363E-10
8	2500	24	1.8118E-10	1.8122E-10	1.8124E-10	1.8121E-10
9	2500	48	1.8125E-10	1.8129E-10	1.8132E-10	1.8129E-10
10	2500	72	1.8131E-10	1.8138E-10	1.8141E-10	1.8137E-10
11	2500	96	1.8124E-10	1.8127E-10	1.8130E-10	1.8127E-10

The lifetime reliability data were placed on a linear plot, shown in Figure 19, to provide the relationship between the measured capacitance value and the length of time during which the capacitor was stressed. Including the system accuracy of the meter used to measure the capacitance during testing, an error bar is included in this figure to identify a one percent variation in the measured capacitance under testing conditions.

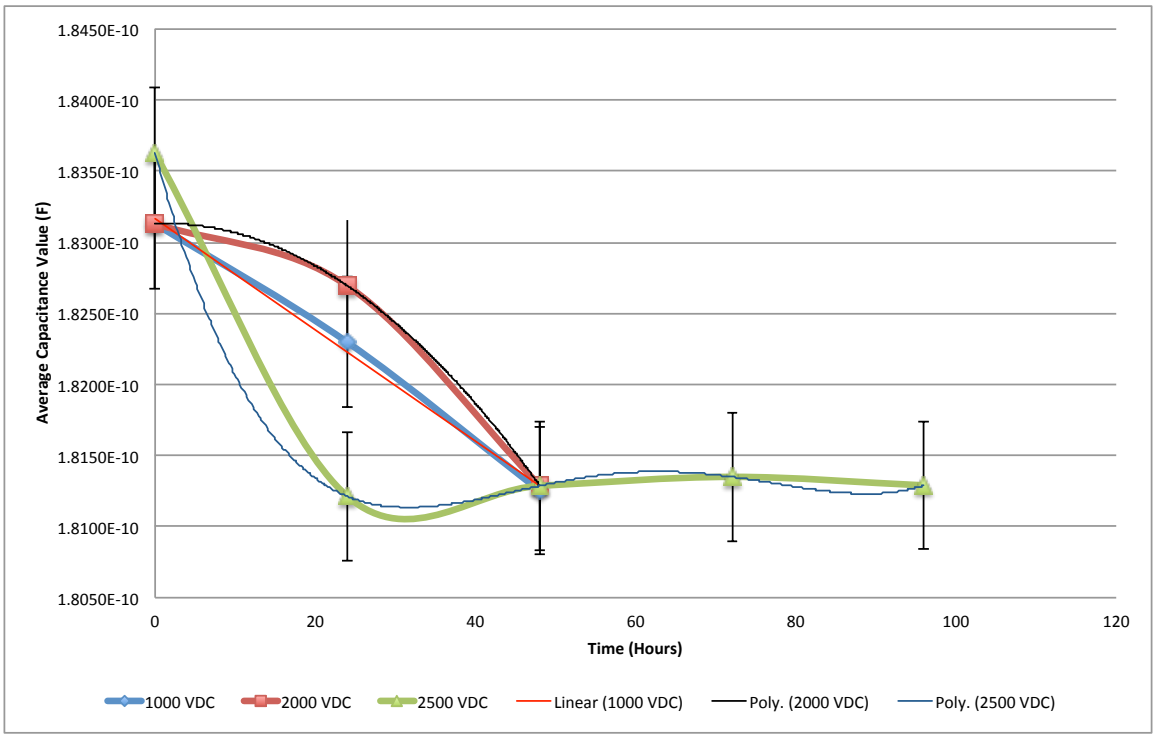

Figure 19. Linear plot of measured capacitance value versus length of time in which the capacitor was stressed. The trend lines used for the extrapolation data come from this plot.

1. Extrapolated Data for Comparison of Lifetime Reliability

Due to equipment issues associated with the software recording the data measurements, the length of time to complete each stress test was severely reduced. To approximate the lifetime reliability of the capacitors, the lifetime reliability data had to be extrapolated from the several data points collected during the testing. The extrapolation method is a proven method used in other lifetime reliability testing when the time allowed for testing is limited. Extrapolated lifetime data is not as accurate as the continued lifetime testing data, but it gives the expected lifetime of the capacitor under similar operating conditions with a certain variance.

The extrapolation method requires the use of a trend line taken from each data set at each test voltage. Using the plotted relationships between the measured capacitance value and the length of time in which the capacitor was stressed from Figure 19, the extrapolated lifetime data, listed in Table 5, was created.

Table 5. Extrapolated capacitance used to compare the measured lifetime reliability to the expected lifetime reliability provided by the capacitor manufacturer.

Test Voltage	R^2 Value	Trendline Equation	Capacitor Lifetime (Years)
1000 VDC	1	$C=-4\ 10^{-14}\ T+2\ 10^{-10}$	8.22
2000 VDC	0.99587	$C = -8\ 10^{-16}T^2 + 2\ 10^{-15}T + 2\ 10^{-10}$	2.15
2500 VDC	1	$C=3\ 10^{-19}T^4 - 7\ 10^{-17}T^3 + 6\ 10^{-15}T^2 - 2\ 10^{-13}T + 2\ 10^{-10}$	0.98

The manufacturer data sheet, which is provided in Appendix B, states that the capacitor lifetime at 1500V DC, and a temperature of 70 degrees Celsius is 11 years. The capacitance value obtained using the extrapolation method for all three stress tests provided a lifetime of less than 11 years.

Due to the limited amount of time to collect the lifetime reliability data, the best fit for these data sets was determined on a case-by-case basis. This was determined using the coefficient of determination, R^2. When R^2 is as close to one as possible, the trend line indicates an accurate representation of the data plotted. For the 1000V DC test, a linear tread line was used due to R^2 being equal to one for this datum set. For the 2000V DC stress condition, a second order polynomial was used since the coefficient of determination, R^2, is as close to one as possible. A fourth order polynomial trend line was determined to be the best fit for the 2500V DC stress testing datum set since R^2 was equal to 1.

From the trend line developed for 1000V DC, an equation was developed, as presented in Table 5. Using the base form of the equation, the equation can be altered to solve for time, T, knowing that a degraded capacitor is classified as a five percent reduction from its original value. Performing this manipulation and knowing our original capacitance value of 180nF leads to

$$T = \frac{1.71\,10^{-10} - 2\,10^{-10}}{-4\,10^{-14}} \rightarrow T = 8.22\ years. \tag{8}$$

Using this same approach, the measured lifetime for 2000V DC and 2500V DC were calculated and are indicated in Table 5.

At 2500V DC, a variation in the capacitance value was observed, as depicted in Figure 19. The capacitance value leveled off at the 48-hour mark and did not decrease as

the capacitor continued to be stressed. This is believed to be an indication of the self-healing process that occurs in thin film capacitors. As noted in Chapter II, when self-healing occurs, a small portion of the total capacitance is removed. This occurs only in areas where material defects are present. For this capacitor, self-healing occurred during the initial 48 hours of testing. Once these material defects were removed, the capacitance value remained constant. The overall change in the capacitance value due to the self-healing is within one percent of the initial value.

Since all of the capacitors tested have the same material properties, it can be said that if time were available, the same trend of self-healing would be visible for the 1000V DC test condition and the 2000V DC condition. Analyzing the test results after the initial 48 hours of testing, the capacitors are relatively robust in design. Once the initial defects are removed due to the self-healing process, the capacitance value is constant even at an elevated temperature and voltage.

The data collected and analyzed during this investigation were presented in this chapter. Concluding remarks and future work in this area are presented in Chapter VI.

VI. CONCLUSIONS AND RECOMMENDATIONS

The conclusions developed from the investigation of the thin film capacitor will be discussed in this chapter and recommendations for future work will be presented.

A. RELIABILITY AND CHARACTERIZATION OF THE THIN FILM CAPACITOR

In this thesis, the characterization of the thin film capacitor was performed and the lifetime reliability of the thin film capacitor used in the IPC AC link converter was investigated.

1. Characterization Concluding Remarks

Treating a thin film capacitor as a semiconductor device proved to be a valid characterization method. The developed IV curves depicted that SCLC does occur in thin film capacitors, and characterization methodology used for semiconductors is also valid for thin film capacitors.

The adverse effects of testing in a noise filled laboratory were also brought to light. The measurements that were required to properly characterize the thin film capacitor had very low signal strength and required multiple circuit design alterations to limit background noise effects. The use of the copper-clad box and air connection method proved to be very helpful when dealing with the excessive noise issue while completing the testing for the characterization of the thin film capacitor.

The development of this alternative characterization method of these capacitors provides a better understanding of their degradation behavior over time at a material science level. These results will also aid in the ability of the DoD to procure the best alternative energy systems available for use on military installations.

2. Lifetime Reliability Concluding Remarks

The thin film capacitor proved to be a very robust design. When taking the self-healing process into consideration, the expected lifetime will be greater than advertised. When a higher voltage is applied, the self-healing process occurs more rapidly, with the

defects states being removed within 48 hours. The lifetime reliability of these capacitors will allow for a greater understanding of how alternative energy system lifetime can be evaluated.

B. FUTURE WORK

This thesis has been the first of this type at the Naval Postgraduate School. Although the lifetime reliability testing and characterization of the thin film capacitor proved to be a worthwhile investigation, future work is needed in both of these areas.

The major issue in characterizing thin film capacitors is due to noise. A future approach would expand on the copper-clad box and air connection method, where the measurements could even be performed in a Faraday cage to minimize external noise. In addition, electron microscopy could also be performed to identify the change in trap concentration after the capacitor is stressed. The traps associated in the manufacturing process could also be identified using electron microscopy to minimize these material defects for future development of the design of the thin film capacitor.

When a higher voltage is applied, the self-healing process occurs more rapidly, with the defects states being removed within 48 hours. A future area to investigate would be to allow for a longer testing period to evaluate if the self-healing occurs within the first 48 hours at all voltages. This will indicate if the material defect concentration is consistent across all the capacitors.

Finally, a future approach for additional reliability testing would be to redesign the support equipment used to reach higher voltages (>2500V DC) or higher temperatures. Testing using AC voltage would also identify any possible differences between AC and DC voltage applications.

APPENDIX A. SAFETY PROCEDURE

This appendix contains the safety procedure that was used for the safe completion of this thesis.

Regulatory excerpt Section 19.16(2) of the *OHS Regulation ("Regulation")* states:

If it is not practicable to completely isolate high voltage electrical equipment,

(a) this document must be adhered to when ever possible.

(b) two or more qualified and authorized persons must be present while the work is being done, unless the procedures being followed under paragraph (a) specifically permit the work to be done by one person,

(c) appropriate electrical protective equipment, including rubber blankets, hoses, hoods, gloves and live line tools must be selected, used, stored, and

(d) the use of metal ladders, wire reinforced side rail wooden ladders, metal scaffolds or metal work platforms must be in accordance with the procedures established under paragraph (a).

Section 4.3 of the *Regulation* states:

(1) The employer must ensure that each tool, machine and piece of equipment in the workplace is

(a) capable of safely performing the functions for which it is used, and

(b) selected, used and operated in accordance with

(i) the manufacturer's instructions, if available,

(ii) safe work practices, and

(iii) the requirements of this Regulation.

(2) Unless otherwise specified by this Regulation, the installation, inspection, testing, repair and maintenance of a tool, machine or piece of equipment must be carried out

(a) in accordance with the manufacturer's instructions and any standard the tool, machine or piece of equipment is required to meet, or

(b) as specified by a professional engineer.

(3) A tool, machine or piece of equipment determined to be unsafe for use must be identified in a manner which will ensure it is not inadvertently returned to service until it is made safe for use.

(4) Unless otherwise specified by this Regulation, any modification of a tool, machine or piece of equipment must be carried out in accordance with

(a) the manufacturer's instructions, if available,

(b) safe work practices, and

(c) the requirements of this Regulation.

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APPENDIX B. DATA SHEETS

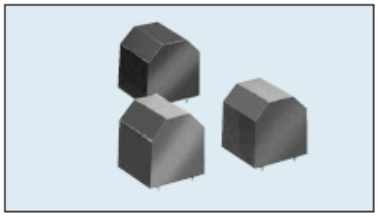
This appendix contains the data sheets for the major equipment used for the completion of this thesis. The first resource, "Capacitor Reliability and Needs," is by A. Ritter of AVX Corporation. The second and third resources are from Stanford Research Systems; the Environmental Chamber is from Sun Electronic Systems and the digital multimeters are by Fluke.

Medium Power Film Capacitors

FAV General Description

TUNING

TUNING



APPLICATIONS

High reactive energy tuning for convertors.
Protection of semi-conductors.

TECHNOLOGY

Metallized polypropylene film and metal foil.
Dry capacitor.

PACKAGING

Rectangular resin case.
4 leads 1.2 x 0.8mm for printed circuit board mounting.
Self-extinguishing plastic case (V0 – in accordance with UL 94) filled thermosetting resin.
Self-extinguishing thermosetting resin (V0 – in accordance with UL 94; I3F2 – in accordance with NF F 16-101).
(Note that FFV3 and FAV3 are in the same packaging.)

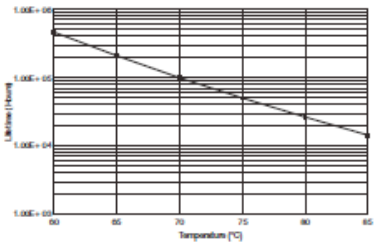
ELECTRICAL CHARACTERISTICS

Climatic category	40/085/56 (IEC 60068)
Working temperature	hot spot temperature: -40°C to +85°C
Hot spot temperature	≤85°C (must be calculated: see below)
Capacitance range C_n	80 to 1200nF
Tolerance	±10%
Rated AC voltage	$V_n$rms – 300 to 650 V
Rated DC voltage	$V_n$dc – 600 to 2000 V
Maximum rms current	Irms max – 10 to 40 Arms
Maximum reactive power	Q max – 7 to 14 kvar
Stray inductance	15 nH
Test voltage between terminals	1.5 x $V_n$dc 10s
Withstanding voltage between terminals and case	3000 Vrms 60s

STANDARDS

IEC 61071-1: IEC 61071-2: Power electronic capacitors
IEC 60068-1: Environmental testing
IEC 60077: Rules for electric traction equipment
UL 94: Fire requirements
NF F 16-101
NF F 16-102: Fire and smoke requirements

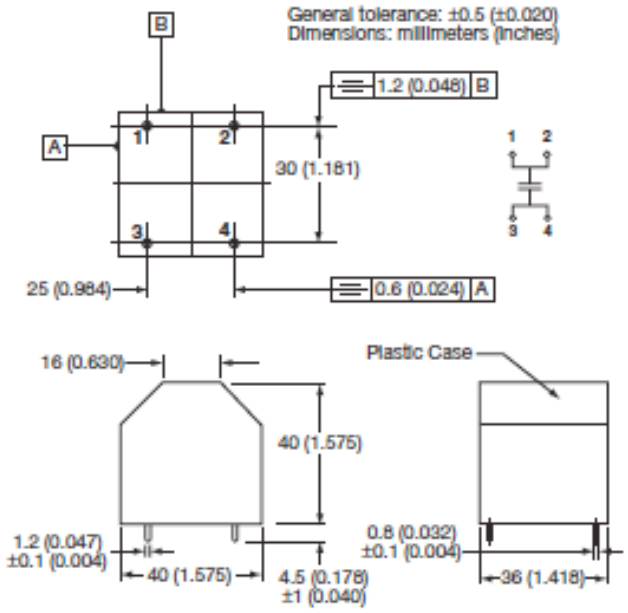
LIFETIME EXPECTANCY



HOT SPOT TEMPERATURE CALCULATION

$\theta_{hot\ spot} = \theta_{ambient} + (P_d + P_l) \times (R_{th} + 7.4)$
with P_d (Dielectric losses) = $Q \times tg\delta_0$
→ [½ x C x $(V_{peak\ to\ peak})^2$ x fr] x 2.10^{-4}
→ Protections applications
→ (V^2 x C x 2 π Fr) x 2.10^{-4}
→ Tuning applications
Pc (Joule losses) = $R_c \times (I_{rms})^2$
where
Q in Var R_c in Ohm R_{th} in °C/W

TUNING



Cn (nF)	I rms max (A)	Q max (kV)	Rs (mΩ)	Ls (nH)	Rth (°C/W)	Part Number
$V_n$dc 600 V	**Vrms: 300 V**					
1200	40	12	0.85	5	4	FAV36KD125K--
1000	32	10	1	5	4.1	FAV36KD105K--
$V_n$dc 800 V	**Vrms: 400 V**					
800	35	14	0.9	5	4	FAV36BD804K--
620	27	11	1.1	5	4.1	FAV36BD624K--
$V_n$dc 1000 V	**Vrms: 450 V**					
560	30	14	1	5	4	FAV36LD564K--
470	25	12	1.2	5	4.1	FAV36LD474K--
$V_n$dc 1200 V	**Vrms: 500 V**					
330	21	11	1.4	5	4.2	FAV36UD334K--
270	17	9	1.7	5	4.4	FAV36UD274K--
$V_n$dc 1500 V	**Vrms: 600 V**					
180	16	10	1.7	5	4.4	FAV36RD184K--
150	13	8	2	5	4.5	FAV36RD154K--
$V_n$dc 2000 V	**Vrms: 650 V**					
120	15	10	1.92.2	5	4.6	FAV36ND124K--
100	12	8	2.8	5	4.9	FAV36ND104K--
80	10	7	1.5	5	5.2	FAV36ND803K--

SERIES PS300 SPECIFICATIONS

General Information

The PS300 series are programmable precision high voltage power supplies for use in laboratory or test applications. They feature reversible polarity, excellent regulation and low output voltage ripple. The digital displays provide accurate readings of voltage and current. Also, digital entry of the current and voltage provides accurate resettability. Output voltage can be set from either the front panel, the remote analog voltage, or over the optional GPIB interface. Voltage and current signals are also available for remote monitoring.

Electrical Specifications

Model	Output Voltage	Maximum Output Current
PS310	12 to ±1250 Volts	20 mA
PS325	25 to ±2500 Volt	10 mA
PS350	50 to ±5000 Volts	5 mA

Voltage Set Accuracy	0.01% + 0.05% of full scale
Voltage Display Accuracy	V Set Accuracy ±1 Volt, typ (±2 Volt, max)
Voltage Resolution	1 Volt (set and display)
Voltage Resettability	1 Volt
Voltage Limit Range	0 to 100% of full scale
Voltage Regulation (*)	Line: 0.001% for ±10% line voltage change Load: 0.005% for 100% load change, typ
Output Ripple	< 0.0015% of full scale, Vrms, typ < 0.002% of full scale, Vrms, max
Current Limit and Trip Range	0 to 105% of full scale
Current Set accuracy	0.01% + 0.05% of full scale
Current Resolution	PS310: 10 µA PS325: 10 µA PS350: 1 µA
Current Display Accuracy	PS350: I Set Accuracy ±1 µA, typ (±2 µA, max) PS325 or PS310: Accuracy ±10 µA, typ (±20 µA, max)
Stability	0.01% per hour, < 0.03% per 8 hours
Temperature Drift	50 ppm / °C, 0° to 50° C, typ
Protection	Arc and short circuit protected; programmable voltage and current limits and current trip.

(*) Regulation specifications apply for > 0.5% (full load) or 1.0% (no load) of full scale Voltage. Below these values the unit may not regulate correctly.

SPECIFICATIONS

SR560 LOW-NOISE PREAMPLIFIER SPECIFICATIONS CHART

Inputs	Single-ended or true differential
Impedance	100 MΩ + 25 pF, DC-coupled
Maximum Inputs	1 VDC before overload; 3 V peak to peak max AC coupled; protected to 100 VDC
Maximum Output	10 Vpp
Noise	<4 nV/√Hz at 1 kHz
CMRR	>90 dB to 1 kHz, decreasing by 6 dB / octave (20 dB / decade) above 1 kHz
Gain	1 to 50,000 in 1-2-5 sequence vernier gain in 0.5% steps
Frequency Response	Gains up to 1000, small signal ±0.5 dB to 1 MHz ±0.3 dB to 300 kHz -3 dB at 1 MHz, 1 Vpp output
Gain Stability	200 ppm /°C
DC Drift	5 μV/°C referred to input (DC coupled)
Filters	0.03 Hz to 1 MHz, 10% typical accuracy
Distortion	0.01% typical
Power	100, 120, 220, 240 VAC (50/60 Hz), 60 Watts Max Internal Batteries: 3 x 12 V, 1.9 Ah sealed lead-acid (rechargeable) ±12 VDC in / out through rear panel banana jacks.
Battery Life	15 hours nominal 250-1000 charge / discharge cycles
Charge Time	4 hours to 80% of capacity
Mechanical	1/2 Rack-Mount width, 3 1/2" height, weight 15 lbs.
Dimensions	14-7/8" x 8-1/8" x 3-1/2"
Warranty	1 year parts and labor on materials and workmanship

ENVIRONMENTAL CHAMBER EC11

- **0.7 FT³ WORKING VOLUME**
- **INTEGRAL USER**
  Temperature Probe
- **LCO_2, -73°C TO +315°C COOLING**
  Optional LN_2, -184°C to +315°C
- **IEEE-488, RS232, RS422**
  Remote Communication
- **EXPANDED I/O ARCHITECTURE**
  Analog Input Ports
  Analog Output Ports
  Auxiliary I/O Drivers
  Digital Parallel Port
  High Speed Serial Link
- **LOCAL TEMPERATURE**
  Controlled Ramping

The EC11 is an advanced environmental chamber intended for automated test system and laboratory applications which require fast temperature cycling. Temperature ramping rates are locally controlled from 0.01°C/sec. The Model EC11 is ideally suited for many forms of MIL-883 testing and other forms of fast temperature cycling testing. Local programs are entered using a BASIC like command set programming language. In automated test systems, the EC11 functions as a remote data acquisition and control system using the capability of its expanded I/O architecture.

The electrically isolated user temperature probe allows for direct monitoring of critical temperatures on the device under test or certain areas inside the test chamber. As well as being displayed on the front panel, readings are accessible from the IEEE-488 or RS232/422 interfaces.

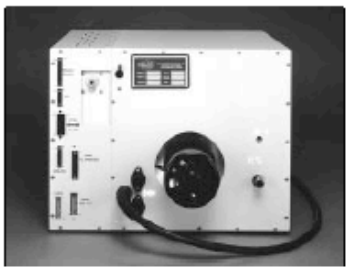
The EC11 command set, whether entered from the local keyboard or downloaded over the IEEE-488 or RS232/422 interfaces, provides for setting chamber temperature, temperature ramping rate and soak time at temperature, temperature deviation limits and temperature upper and lower limits.

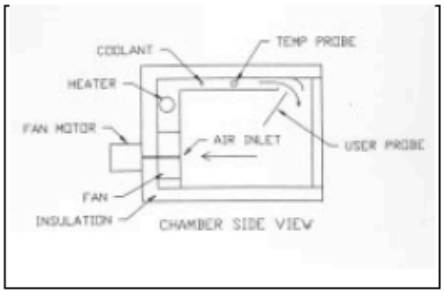
Probe calibration procedures are built into the EC11 using local menu driven format. Special communication commands allow for communication to the analog I/O ports, the high speed serial port (SPI) and the parallel port. The chamber can be controlled remotely from the RS232/422 port or the IEEE-488 bus interface. When the IEEE-488 bus interface is used, transparent communication from the IEEE-488 bus to the RS232/422 port is supported. Programs and parameters are stored in battery-backed memory.

The PID coefficients used in the EC11 are user adjustable from the keyboard and remote interfaces. In addition, alarm function and sound level, BAUD rate, interrupt assignments and other communication port options are configurable from the front panel using an easy, menu driven format.

The EC11 supports several safety features including a mechanically adjustable over temperature thermostat, upper and lower software temperature limits, processor watchdog timer and open and short probe detection.

The EC11 is designed to be adaptable to your system application. If you have special requirements, call Sun Systems for solutions.





Sun Electronic Systems, Inc. Titusville, FL 32780
Tel:(321) 383-9400 · Fax: (321) 383-9412
Email: info@sunelectronics.com
Web: www.sunelectronics.com

GENERAL SPECIFICATIONS *(subject to change without notice)*

MECHANICAL

Internal Dimensions	(30.5cmW x 24.75cmH x 26.0cmD)	12.0"W x 9.75"H x 10.25"D
Test Volume	(0.020m³)	0.7ft³
Overall Dimensions	(53.3cmW x 40.6cmH x 61.0cmD)	21.0"W x 16.0"H x 24.0"D
Exterior Construction		Painted Aluminum Alloy
Door (see options)		Blank door supplied with chamber
Interior Construction		Stainless Steel, with exhaust port
Coolant Input		LCO_2, 37° male fitting, 1/4" tube
		(optional) LN_2, 45° male fitting, 1/2" tube
Exhaust		3/8" NPT, male
Weight	(22 kg typical; 31 kg shipping)	49 lbs typical; 68 lbs shipping

PERFORMANCE

Set Temperature Range (LCO_2)	(-100°F to +600°F)	-73°C to +315°C
With LN_2 Option	(-300°F to +600°F)	-184°C to +315°C
Temperature Ramping Rate Range (Heating and Cooling)	(0.02°F to 86°F/min)	0.01°C to 48°C/min
Number of Programmable Temperature Setpoints		Typically 100+
Time at Temperature Setpoint Range		1.0 sec to 99 hr, 59 min, 59 sec
Number of Programmable Set Times		Typically 100+
Air Circulation		120 CFM, vertical
Absolute Error Over Temp Range (not including probe error)..	(±0.9°F)	±0.5°C
Temperature Resolution (approx.)	(0.04°F)	0.02°C
Long Term Stability (per month)	(±0.4°F)	±0.2°C
Line Voltage Sensitivity	(±0.2°F)	±0.1°C for ± 10% Line Voltage Change
Temperature Control Technique		Dual PID Algorithm, PWM
Ambient Temperature Operating Range	(32°F to 122°F)	0°C to 50°C
Local Control		29 Key Keyboard (2 Line LCD Display)
Remote Control		RS232 / RS422 / IEEE-488 bus
IEEE-488 to RS232/RS422		Software/Bidirectional Transparent Operation

SAFETY

Line Voltage Dropout	Program and Parameters Stored in Battery Backed Memory (Programmable Automatic Restart after Power Loss)
Fail Safe	Open/Short Probe Detection, Watch-dog Timer, Software Temperature Limits, Over-temperature Thermostat

ELECTRICAL

Heating Input	3600 Watts
Power Requirements	4200 Watts max, 220 VAC, 50/60 Hz, 1 phase Optional 240 VAC (see Options)

Sun Electronic Systems, Inc. Titusville, FL 32780

Tel:(321) 383-9400 • Fax: (321) 383-9412
Email: info@sunelectronics.com
Web: www.sunelectronics.com

FLUKE®

Fluke 8845A/8846A Digital Multimeters

Extended Specifications

The Fluke 8845A and 8846A 6.5 digit precision multimeters have the precision and versatility to handle your most demanding measurements, on the bench or in a system. These meters are both high performance and feature rich, yet also remarkably easy to use.

Features at a glance

- 6.5 digit resolution
- Basic V dc accuracy of up to 0.0024 % (1 yr.)
- Dual display
- 100 µA to 10 A current range, with up to 100 pA resolution
- Wide ohms ranges from 10 Ω to 1 GΩ with up to 10 µΩ resolution
- 2 x 4 ohms 4-wire measurement technique
- Both models measure frequency and period
- 8846A also measures capacitance and temperature
- USB memory drive port (8846A)
- Fluke 45 and Agilent 34401A emulation
- Graphical display
- Trendplot™ paperless recorder mode, statistics, histogram
- CAT I 1000 V, CAT II 600 V

These digital multimeters perform the functions you would expect to see in a multifunction DMM, including measuring volts, ohms, and amps, with performance that exceeds expectations. Basic V dc accuracy of up to 0.0024 %, 10 A current range, and a wide ohms range from 10 Ω to 1 GΩ with up to 10 µΩ resolution give you an unbeatable combination of measurement capability.

You can also use the 8845A and 8846A to measure temperature, capacitance, period, and frequency—the functions of a counter, capacitance meter, and thermometer are built in for unparalleled versatility. Extend the meters' utility even more with their graphical display modes, including Trendplot™ paperless recorder mode, statistics and histograms—features you won't find on other multimeters.

Of course, these meters are also durable and dependable, features you expect from any Fluke meter. This unique combination of features and performance makes the 8845A and 8846A an unbeatable value for a wide variety of applications, including manufacturing test, research and development, and service.

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